

Compal Confidential

HCW50 Schematics Document

AMD/Sempron/ATI RX485/SB460 W/s M52/54/56P

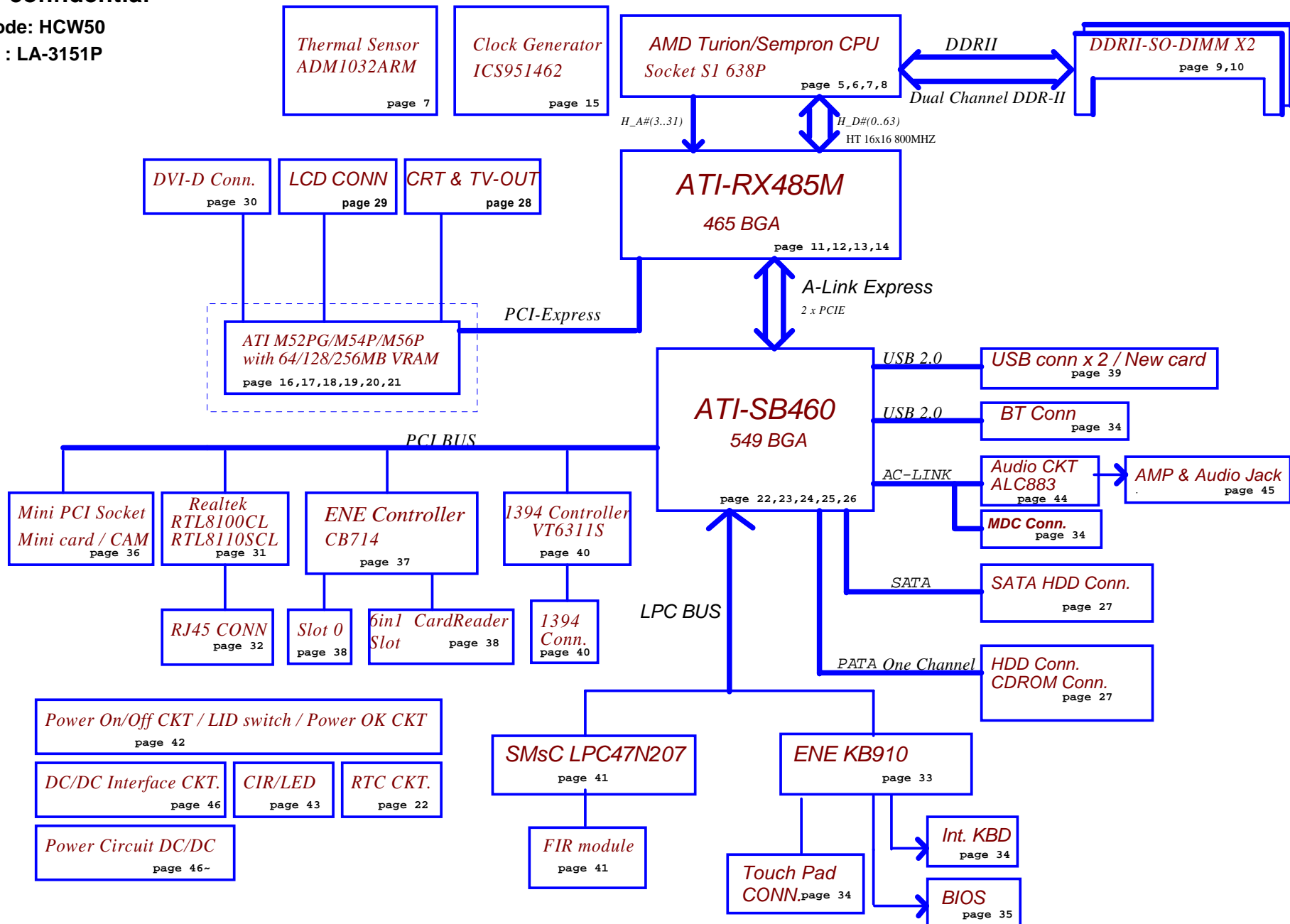
2006 / 02 / 28 Rev:0.3 (For PVT)

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Issued Date		2005/05/09		Deciphered Date		
		2006/03/08		Title		
				SCHEMATIC, M/B LA-3151P		
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Project Code: HCW50

File Name : LA-3151P



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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDRII terminator	ON	ON	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON*
+1.2VS	1.2V switched power rail for PCIE	ON	OFF	OFF
+0.9VS	0.9V switched power rail for VRAM terminator	ON	OFF	OFF
+1.8VALW	1.8V switched power rail	ON	ON	ON*
+VDD_CORE	1.0~1.2V switched power rail for VGA	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQE/PIRQH
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

SB460 SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
VGA	
UMA	
UMA's DVI	
LAN(10/100)	
LAN(GIGA)	
MINI CARD1	
MINI CARD2	
SATA-to-IDE	
PATA	
GRAPEVINE	
G72MV Only	
G73 Only	
VRAM	
VRAM 64M	
VRAM 128M	
VRAM 256M	
MEDIA/B	
CIR	
FIR	
GENEVA	
LCM	
Sub-woofer	

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<11> H_CADIP[0..15] H_CADIP[0..15]
<11> H_CADIN[0..15] H_CADIN[0..15]

H_CADOP[0..15] H_CADON[0..15] <11>
H_CADON[0..15] H_CADON[0..15] <11>

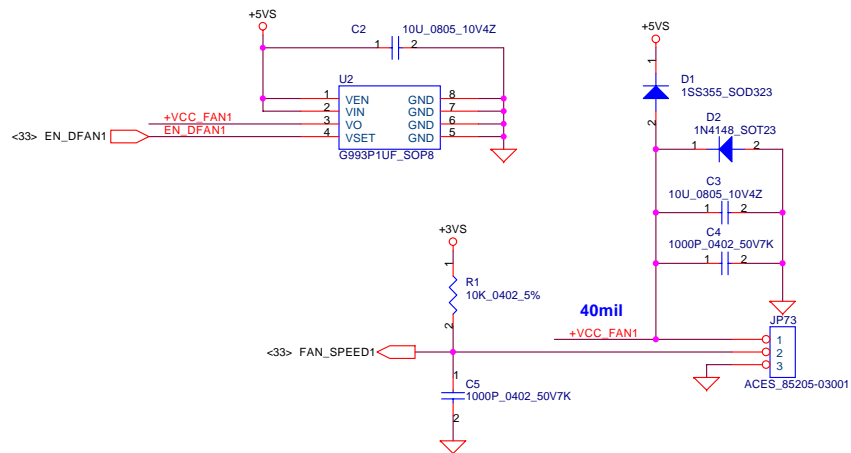
PROCESSOR HYPERTRANSPORT INTERFACE

VLDLT_Ax AND VLDLT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Athlon 64 S1
Processor Socket

FAN1 Conn

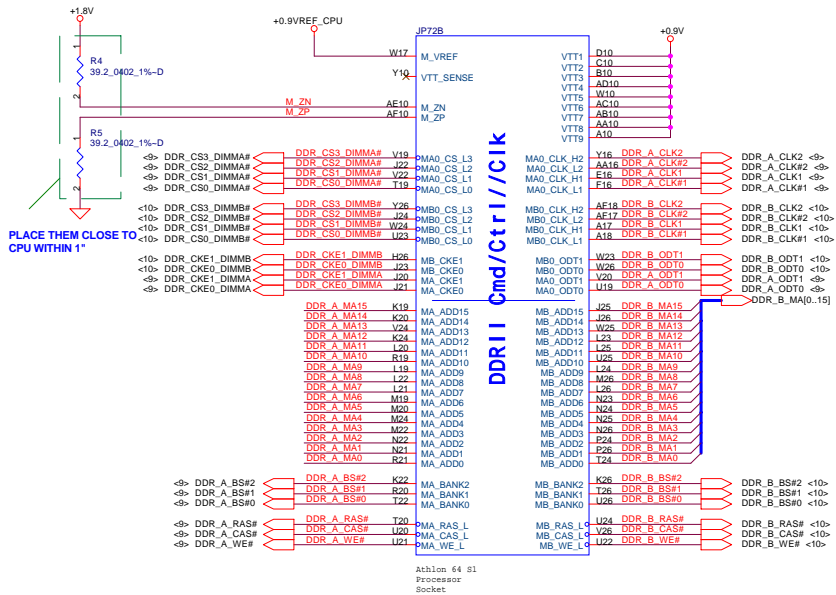


LAYOUT: Place bypass cap on topside of board

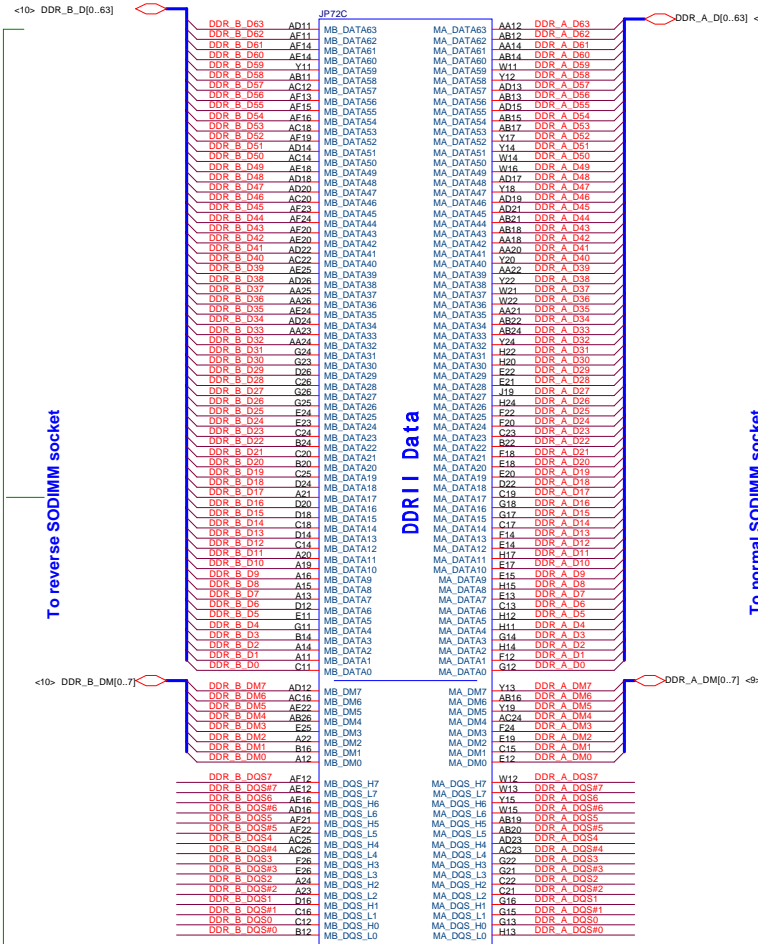
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDLT0 POWER PINS

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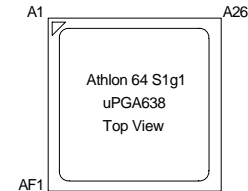
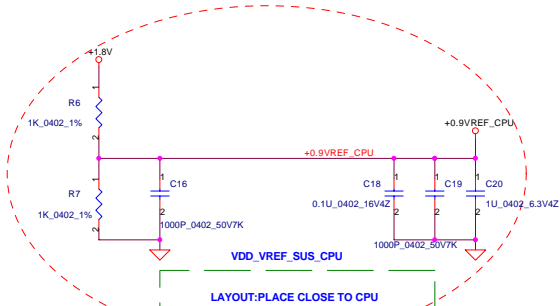
VDD VTT SUS CPU IS CONNECTED TO THE VDD VTT SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE.



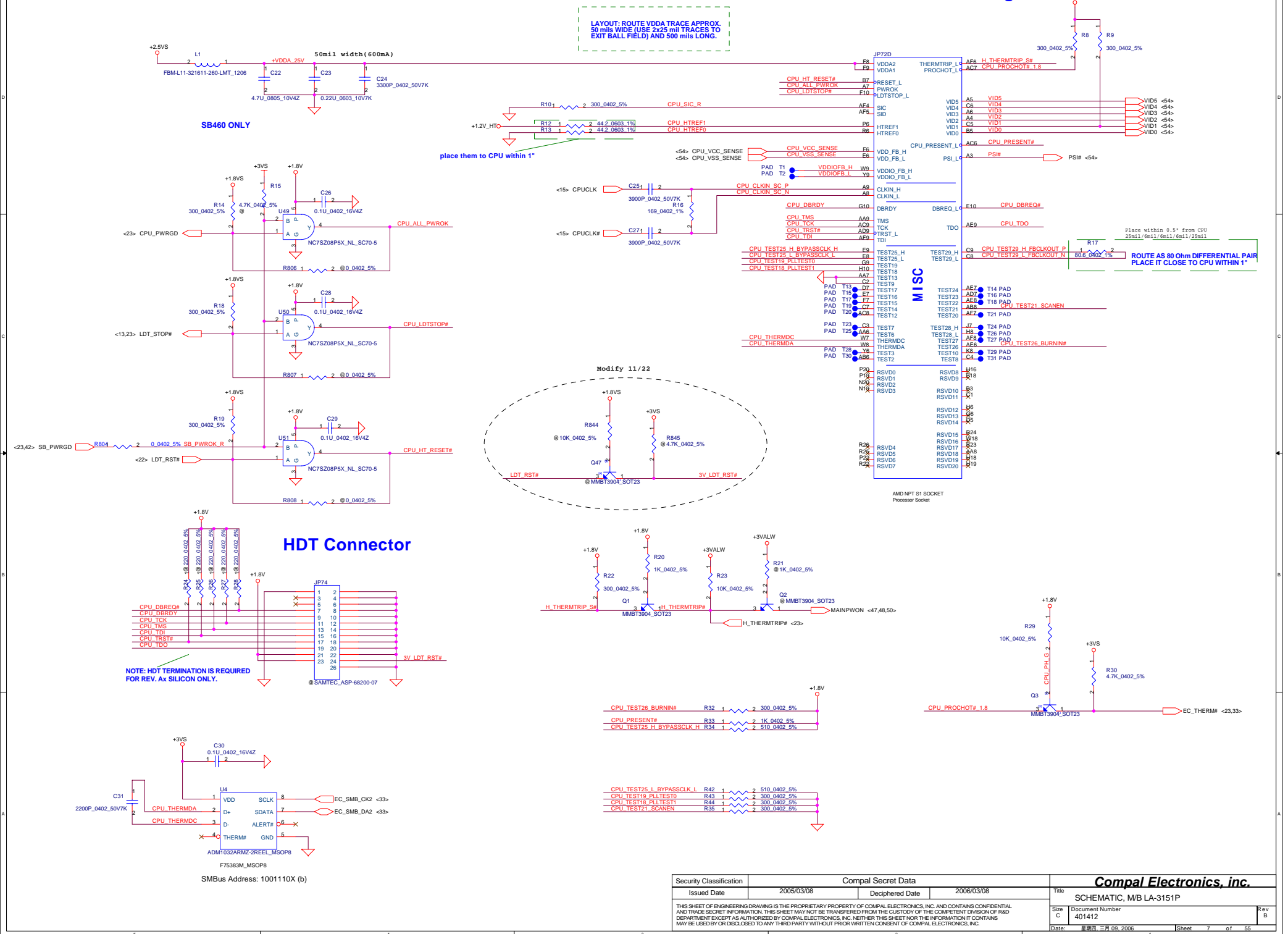
Processor DDR2 Memory Interface

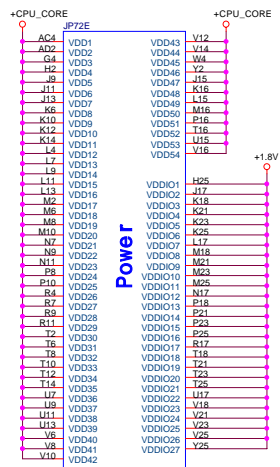


ATI check , Use +0.9V PWR , can delete or not

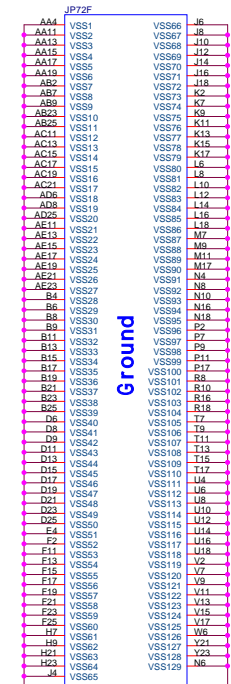
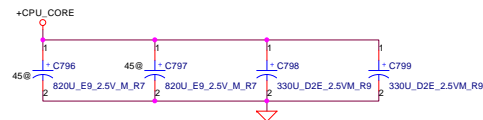


ATHLON Control and Debug

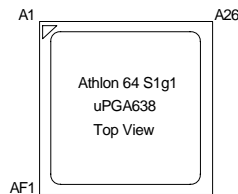




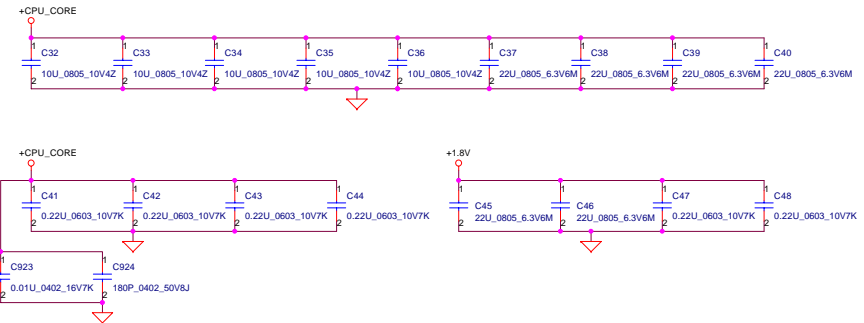
Athlon 64 S1
Processor Socket



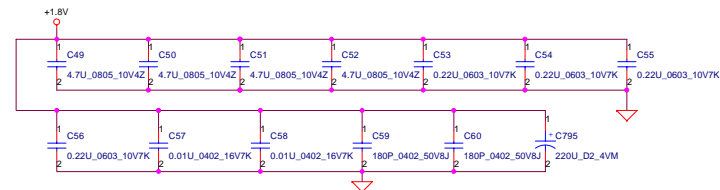
Athlon 64 S1
Processor Socket



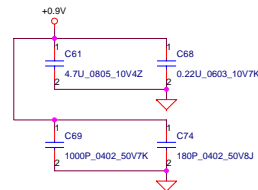
BOTTOMSIDE DECOUPLING



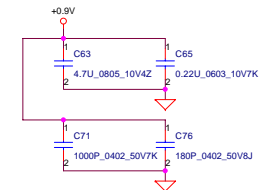
DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



CPU left-hand side



CPU right-hand side



PROCESSOR POWER AND GROUND

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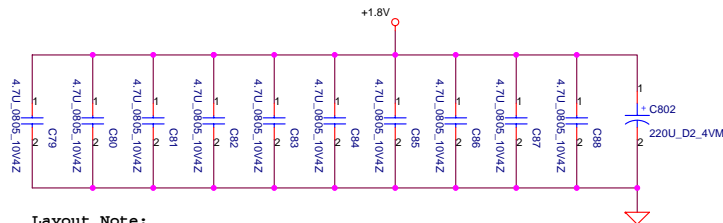
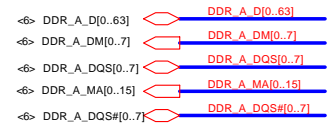
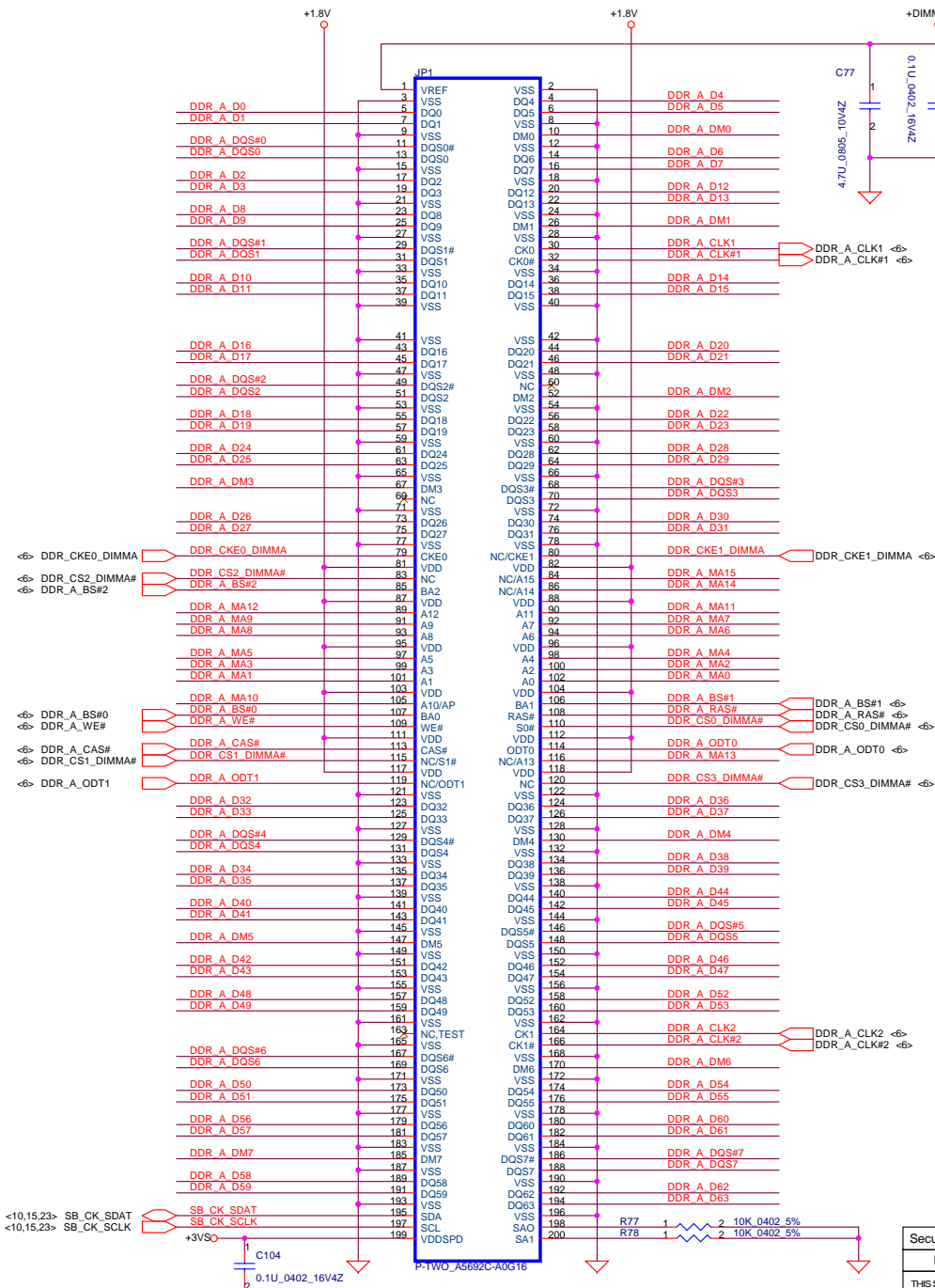
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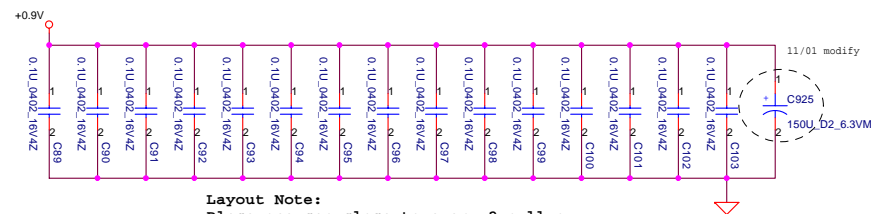
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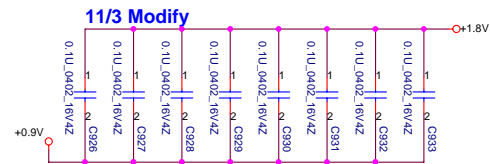
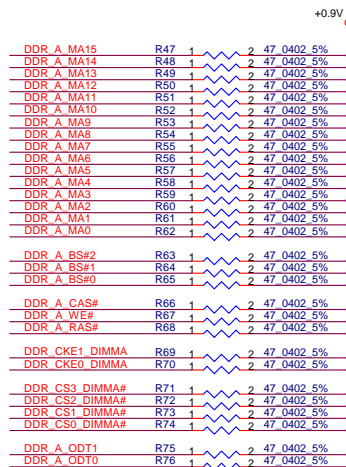
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Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V

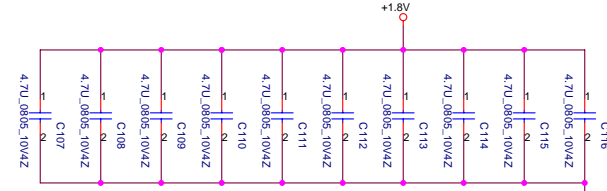
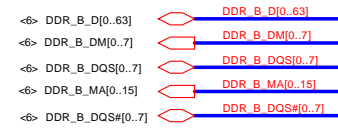
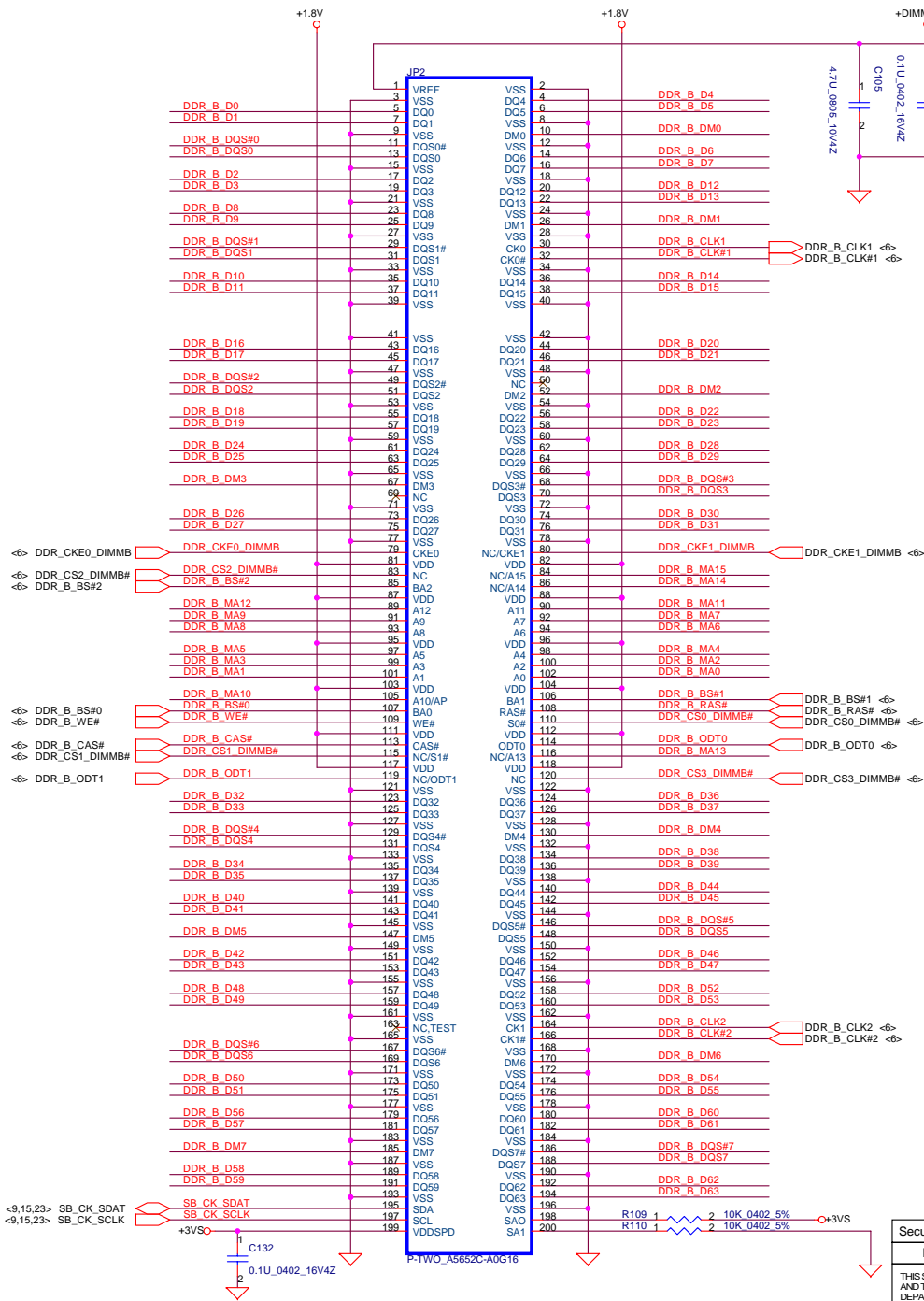


Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V

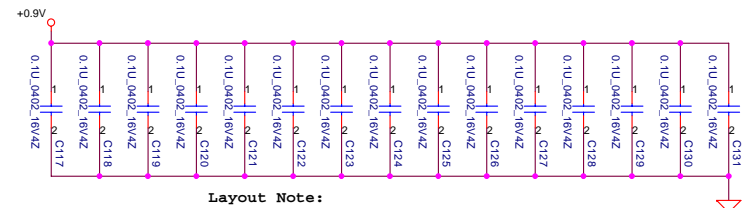


Layout Note:
Place one 0.1uF cap close to every 2 pullup
resistors terminated to +0.9V

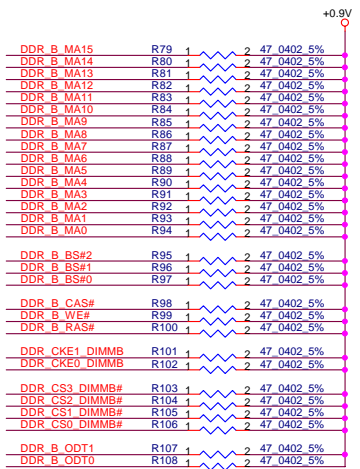
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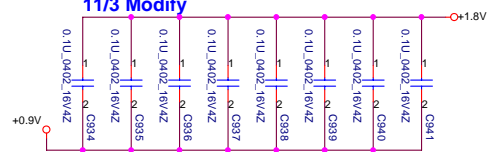
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



11/3 Modify



Layout Note:
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

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<16> PCIE_GTX_C_MRX_P[0..15] PCIE GTX C MRX P[0..15]
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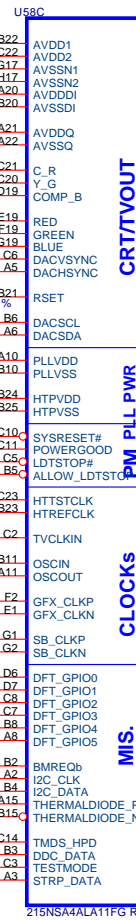
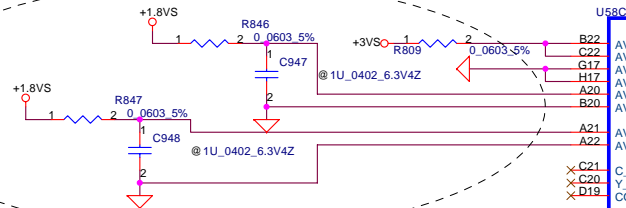
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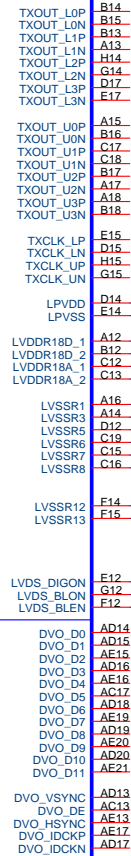
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ATI check , CRT / TV/ LVDS can delete or not when I use RX485

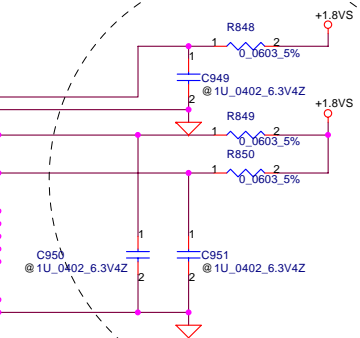
Modify 11/29



PART 3 OF 5



Modify 11/29

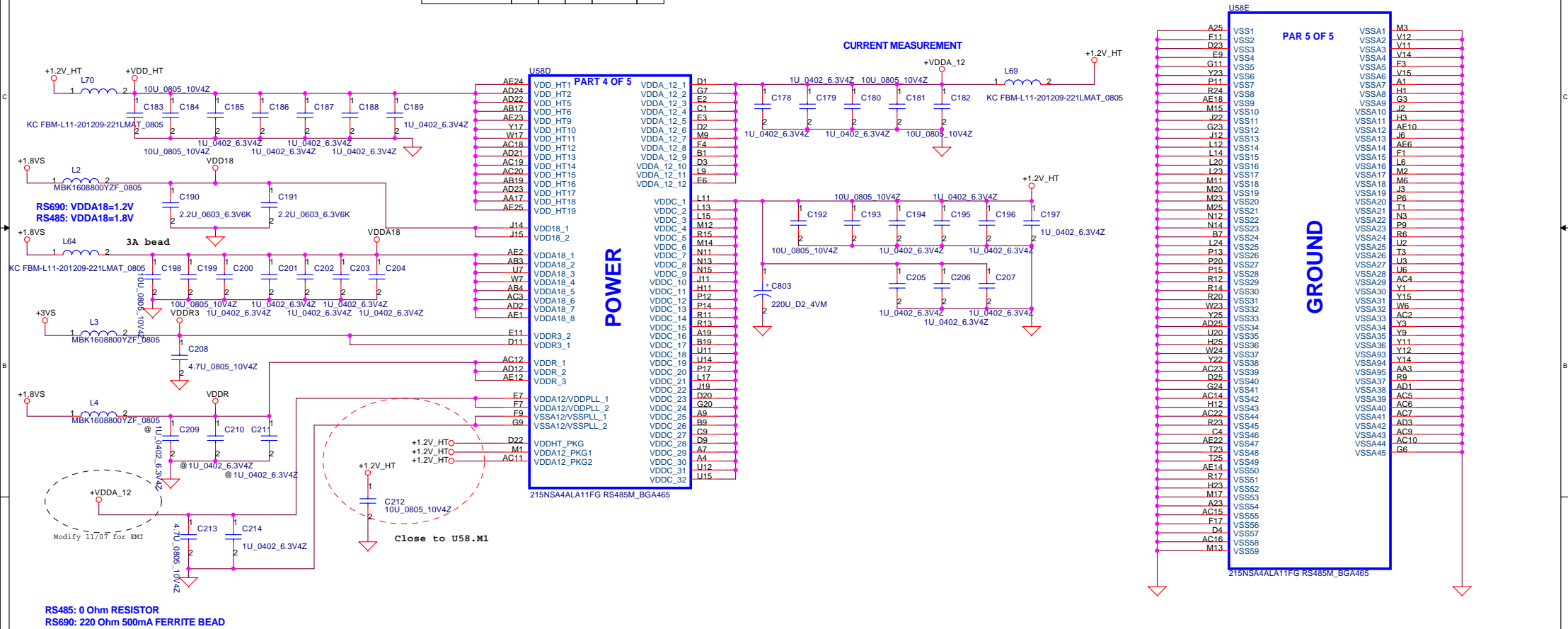


LOAD_ROM#: LOAD ROM STRAP ENABLE

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

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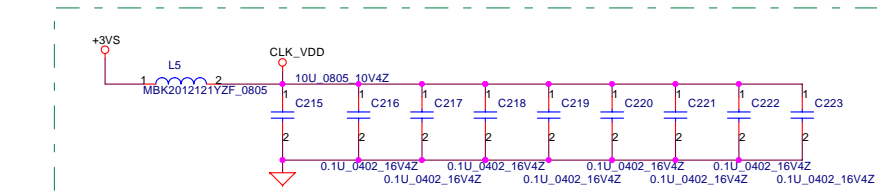
NB RS485 POWER STATES						
Power	Signal	S0	S1	S3	S4/S5	G3
	VDDHT	ON	ON	OFF	OFF	OFF
	VDDR	ON	ON	OFF	OFF	OFF
	VDD18	ON	ON	OFF	OFF	OFF
	VDDC	ON	ON	OFF	OFF	OFF
	VDDA18	ON	ON	OFF	OFF	OFF
	VDDA12	ON	ON	OFF	OFF	OFF
	AVDD	ON	ON	OFF	OFF	OFF
	AVDDDI	ON	ON	OFF	OFF	OFF
	PLLVD	ON	ON	OFF	OFF	OFF
	HTPVDD	ON	ON	OFF	OFF	OFF
	VDDR3	ON	ON	OFF	OFF	OFF
	LPVDD	ON	ON	OFF	OFF	OFF
	LVDDR18D	ON	ON	OFF	OFF	OFF
	LVDDR18A	ON	ON	OFF	OFF	OFF



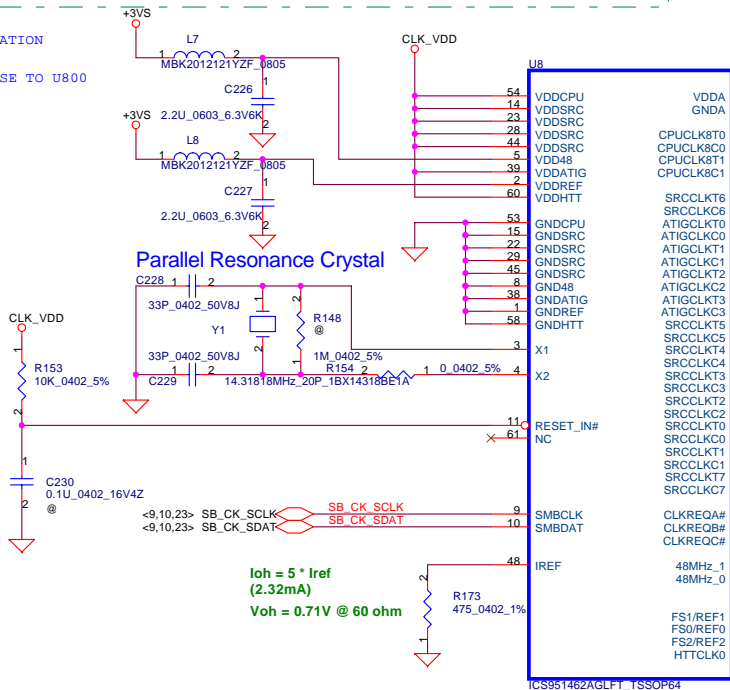
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- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



Parallel Resonance Crystal



$I_{oh} = 5 * I_{ref}$
(2.32mA)
 $V_{oh} = 0.71V @ 60 ohm$

<36,39> ICH_SMBDATA ICH_SMBDATA R192 1 2 0.0402 5% SB_CK_SDAT
<36,39> ICH_SMBCLK ICH_SMBCLK R193 1 2 0.0402 5% SB_CK_SCLK

EXT CLK FREQUENCY SELECT TABLE(MHZ)

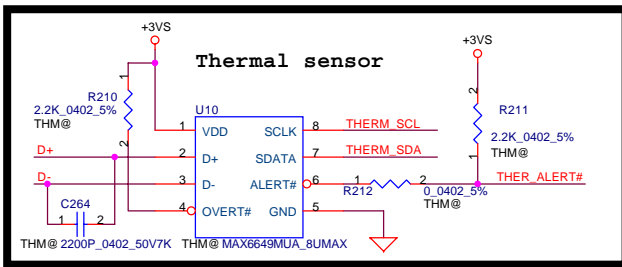
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HIT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

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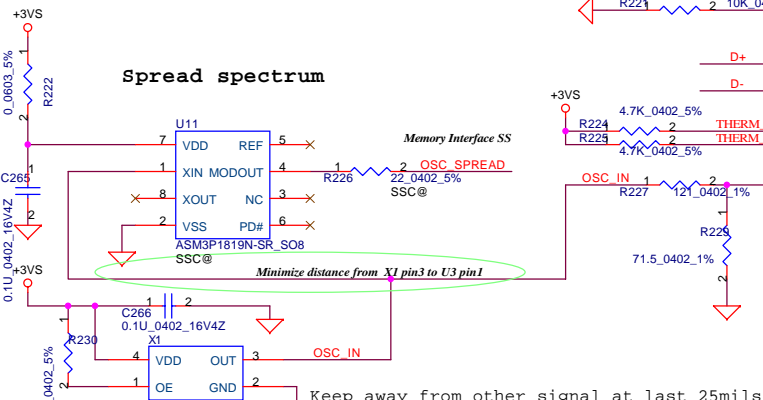
PCIE Lane Reversal

PCIE GTX C MRX N15	C232	2	0.1U 0402 16V7K	PCIE GTX MRX N15	AK27
PCIE GTX C MRX P15	C233	2	0.1U 0402 16V7K	PCIE GTX MRX P15	AK27
PCIE GTX C MRX N14	C234	2	0.1U 0402 16V7K	PCIE GTX MRX N14	AK27
PCIE GTX C MRX P14	C235	2	0.1U 0402 16V7K	PCIE GTX MRX P14	AK27
PCIE GTX C MRX N13	C236	2	0.1U 0402 16V7K	PCIE GTX MRX N13	AK28
PCIE GTX C MRX P13	C237	2	0.1U 0402 16V7K	PCIE GTX MRX P13	AK28
PCIE GTX C MRX N12	C238	2	0.1U 0402 16V7K	PCIE GTX MRX N12	AK27
PCIE GTX C MRX P12	C239	2	0.1U 0402 16V7K	PCIE GTX MRX P12	AK27
PCIE GTX C MRX N11	C240	2	0.1U 0402 16V7K	PCIE GTX MRX N11	AK28
PCIE GTX C MRX P11	C241	2	0.1U 0402 16V7K	PCIE GTX MRX P11	AK28
PCIE GTX C MRX N10	C242	2	0.1U 0402 16V7K	PCIE GTX MRX N10	AK28
PCIE GTX C MRX P10	C243	2	0.1U 0402 16V7K	PCIE GTX MRX P10	AK28
PCIE GTX C MRX N9	C244	2	0.1U 0402 16V7K	PCIE GTX MRX N9	AK27
PCIE GTX C MRX P9	C245	2	0.1U 0402 16V7K	PCIE GTX MRX P9	AK27
PCIE GTX C MRX N8	C246	2	0.1U 0402 16V7K	PCIE GTX MRX N8	AK28
PCIE GTX C MRX P8	C247	2	0.1U 0402 16V7K	PCIE GTX MRX P8	AK28
PCIE GTX C MRX N7	C248	2	0.1U 0402 16V7K	PCIE GTX MRX N7	AK28
PCIE GTX C MRX P7	C249	2	0.1U 0402 16V7K	PCIE GTX MRX P7	AK28
PCIE GTX C MRX N6	C250	2	0.1U 0402 16V7K	PCIE GTX MRX N6	AK27
PCIE GTX C MRX P6	C251	2	0.1U 0402 16V7K	PCIE GTX MRX P6	AK27
PCIE GTX C MRX N5	C252	2	0.1U 0402 16V7K	PCIE GTX MRX N5	AK28
PCIE GTX C MRX P5	C253	2	0.1U 0402 16V7K	PCIE GTX MRX P5	AK28
PCIE GTX C MRX N4	C254	2	0.1U 0402 16V7K	PCIE GTX MRX N4	AK28
PCIE GTX C MRX P4	C255	2	0.1U 0402 16V7K	PCIE GTX MRX P4	AK28
PCIE GTX C MRX N3	C256	2	0.1U 0402 16V7K	PCIE GTX MRX N3	AK27
PCIE GTX C MRX P3	C257	2	0.1U 0402 16V7K	PCIE GTX MRX P3	AK27
PCIE GTX C MRX N2	C258	2	0.1U 0402 16V7K	PCIE GTX MRX N2	AK28
PCIE GTX C MRX P2	C259	2	0.1U 0402 16V7K	PCIE GTX MRX P2	AK28
PCIE GTX C MRX N1	C260	2	0.1U 0402 16V7K	PCIE GTX MRX N1	AK28
PCIE GTX C MRX P1	C261	2	0.1U 0402 16V7K	PCIE GTX MRX P1	AK28
PCIE GTX C MRX N0	C262	2	0.1U 0402 16V7K	PCIE GTX MRX N0	AK27
PCIE GTX C MRX P0	C263	2	0.1U 0402 16V7K	PCIE GTX MRX P0	AK27

<12> PCIE_GTX_C_MRX_P[0..15] <PCIE GTX C MRX P[0..15]>
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Spread spectrum



PCIE MTX C GRX N15	AJ31
PCIE MTX C GRX P15	AH31
PCIE MTX C GRX N14	AH30
PCIE MTX C GRX P14	AG30
PCIE MTX C GRX N13	AG32
PCIE MTX C GRX P13	AF32
PCIE MTX C GRX N12	AF31
PCIE MTX C GRX P12	AE31
PCIE MTX C GRX N11	AE30
PCIE MTX C GRX P11	AD30
PCIE MTX C GRX N10	AD32
PCIE MTX C GRX P10	AC32
PCIE MTX C GRX N9	AC31
PCIE MTX C GRX P9	AB31
PCIE MTX C GRX N8	AB30
PCIE MTX C GRX P8	AA30
PCIE MTX C GRX N7	AA32
PCIE MTX C GRX P7	Y32
PCIE MTX C GRX N6	Y31
PCIE MTX C GRX P6	W31
PCIE MTX C GRX N5	W30
PCIE MTX C GRX P5	V30
PCIE MTX C GRX N4	U32
PCIE MTX C GRX P4	U31
PCIE MTX C GRX N3	T31
PCIE MTX C GRX P3	T30
PCIE MTX C GRX N2	R32
PCIE MTX C GRX P2	R31
PCIE MTX C GRX N1	P32
PCIE MTX C GRX P1	P31
PCIE MTX C GRX N0	N31

U9A

GPIO

GPIO_0

GPIO_1

GPIO_2

GPIO_3

GPIO_4

GPIO_5

GPIO_6

GPIO_7

GPIO_8

GPIO_9

GPIO_10

GPIO_11

GPIO_12

GPIO_13

GPIO_14

GPIO_15

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GPIO_192

GPIO_193

GPIO_194

GPIO_195

GPIO_196

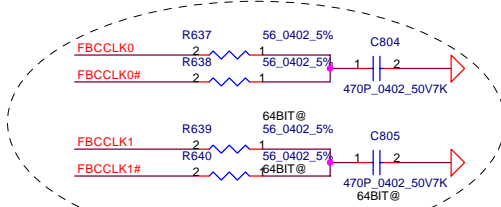
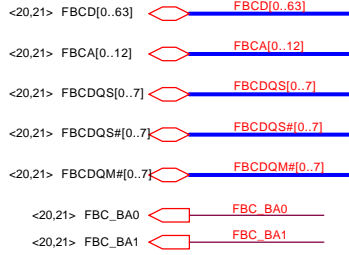
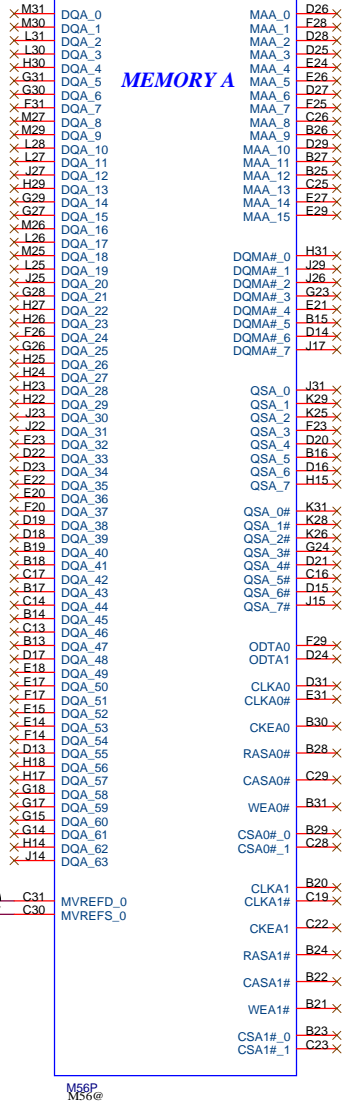
GPIO_197

GPIO_198

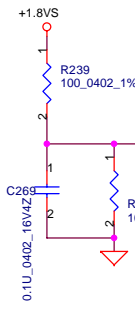
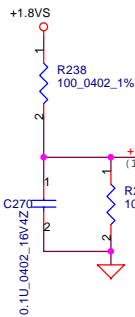
GPIO_199

GPIO_200

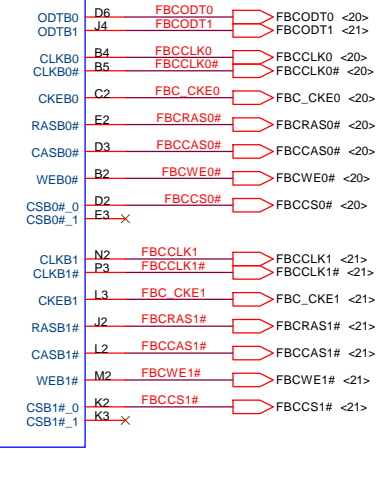
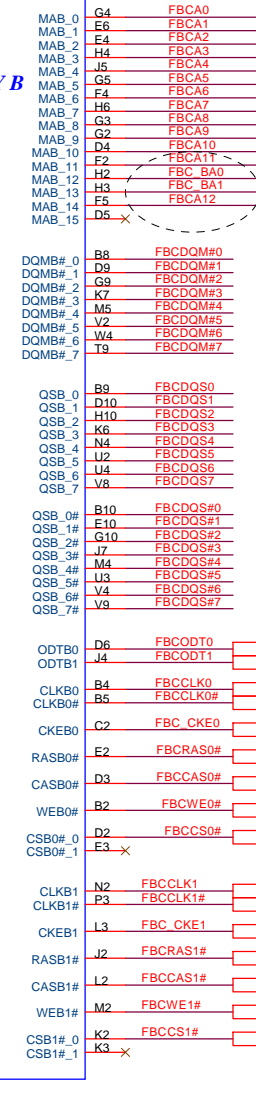
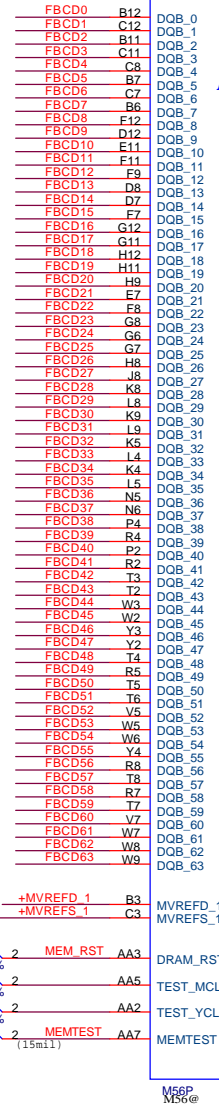
MEMORY A



10/20/05"
Close to Memory Side



MEMORY B



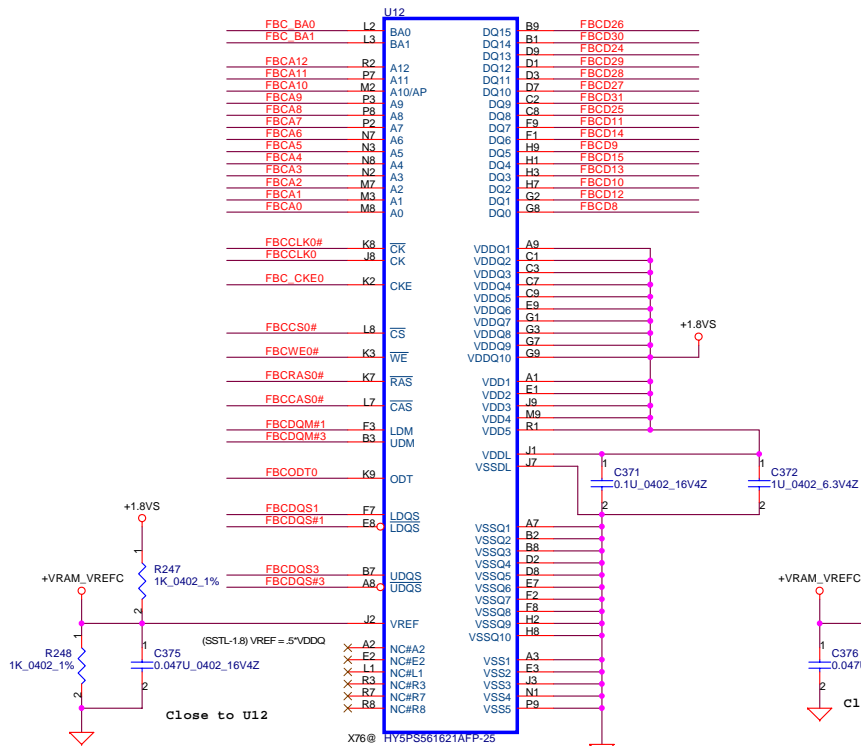
GDDR2

WWW.AliSaler.Com

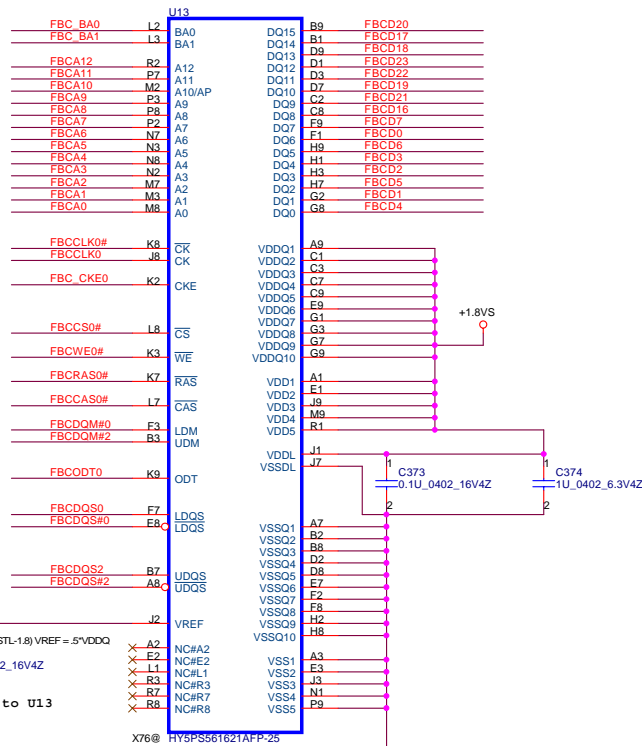
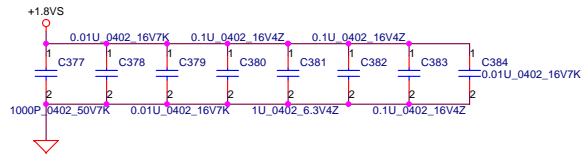
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11/03/05' SWAP NET
11/04/05' SWAP NET
11/08/05' SWAP NET

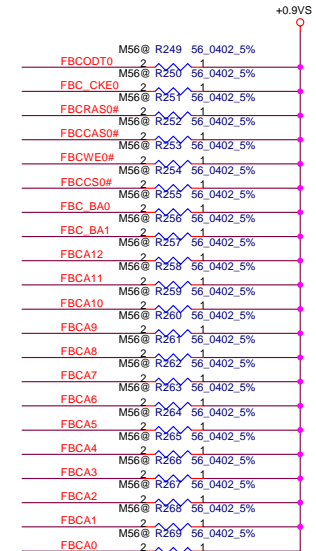
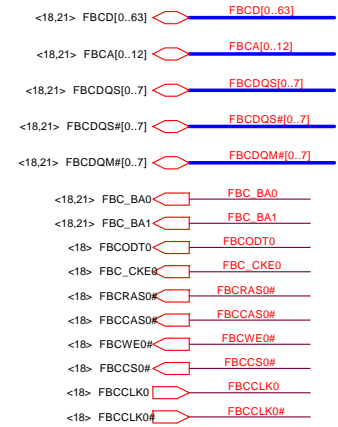
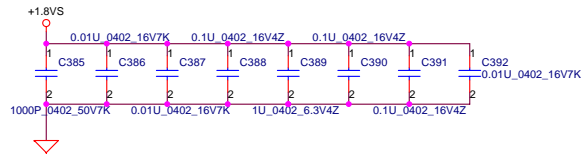
11/03/05' SWAP NET



DDR2 BGA MEMORY

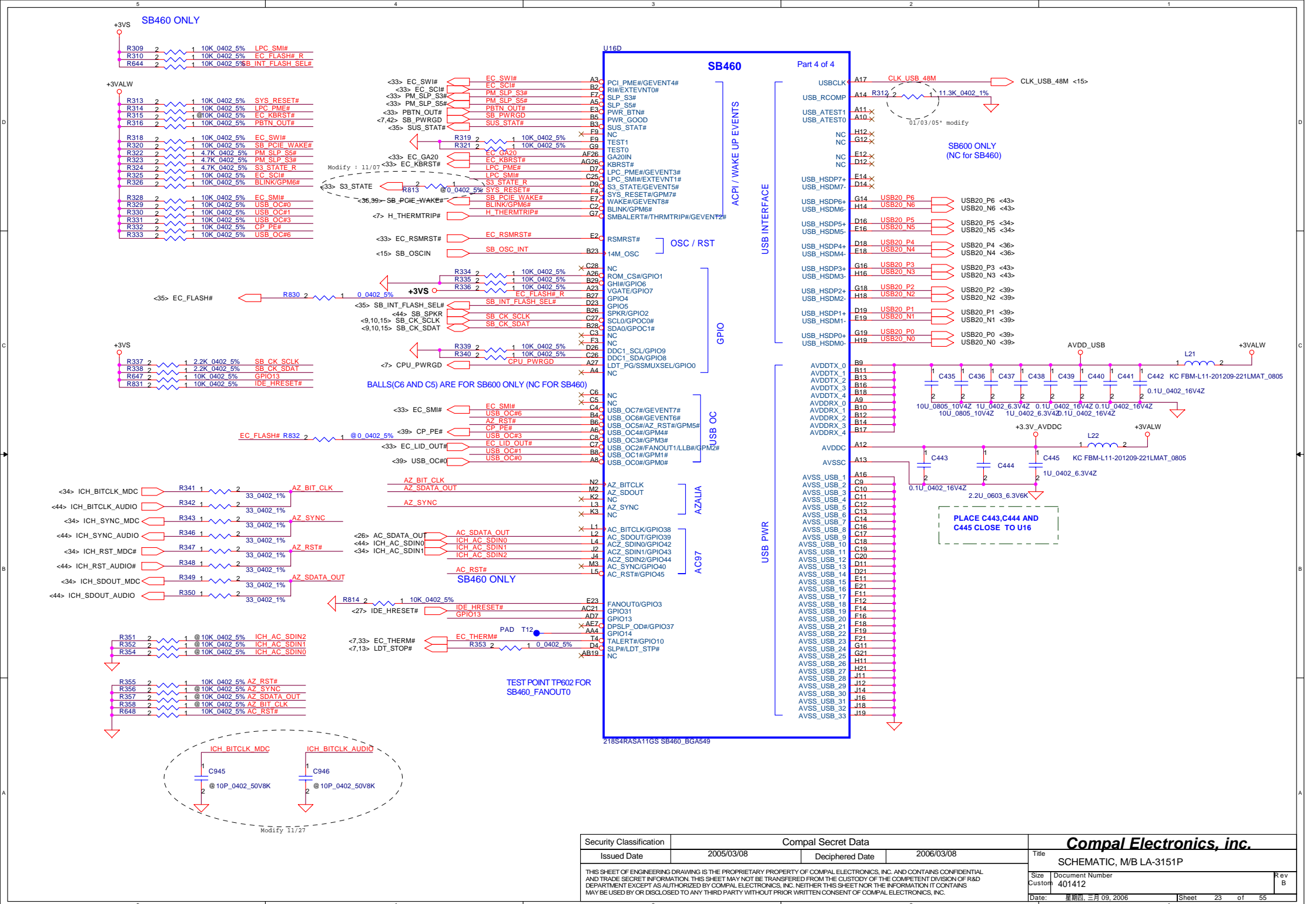


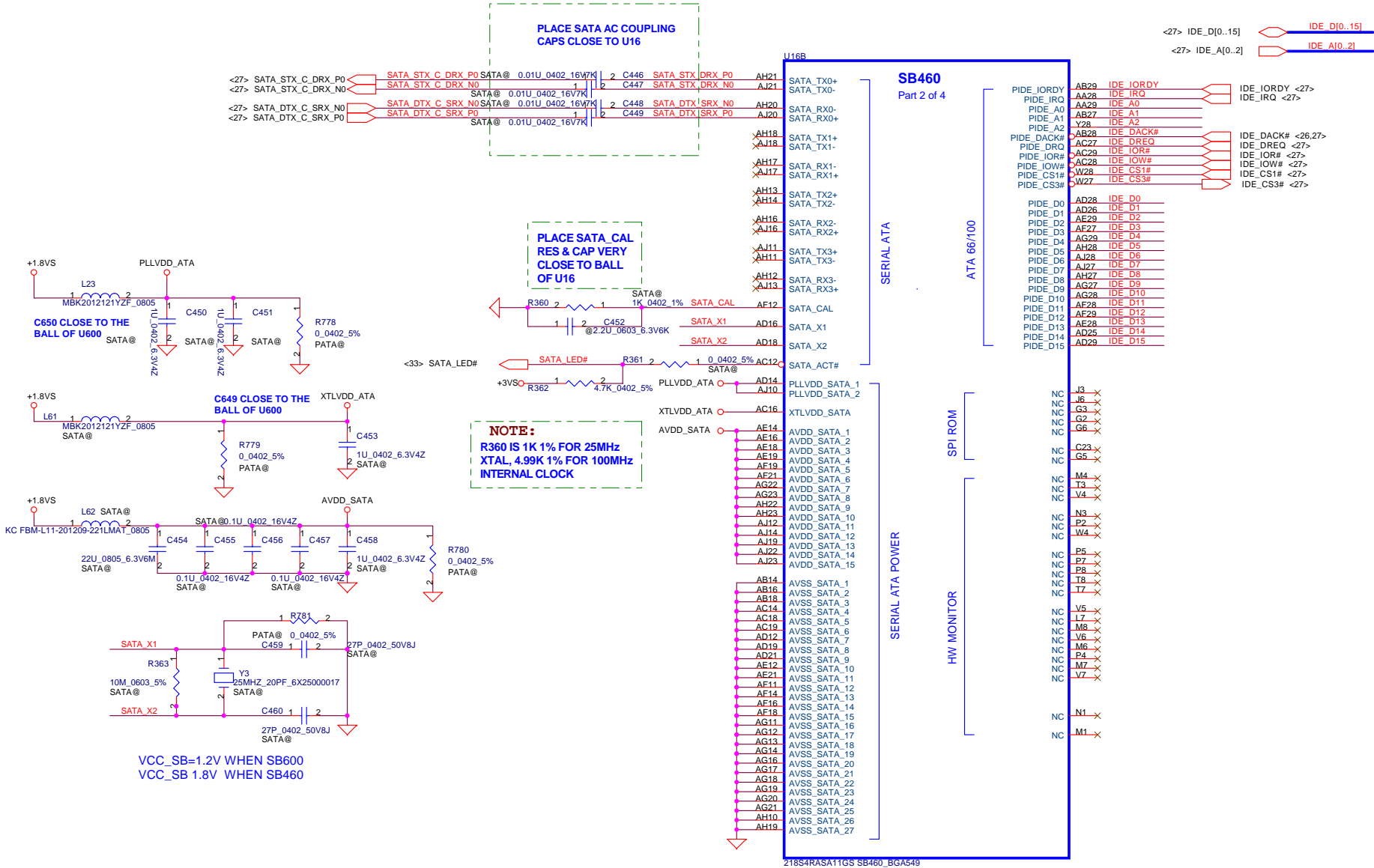
DDR2 BGA MEMORY



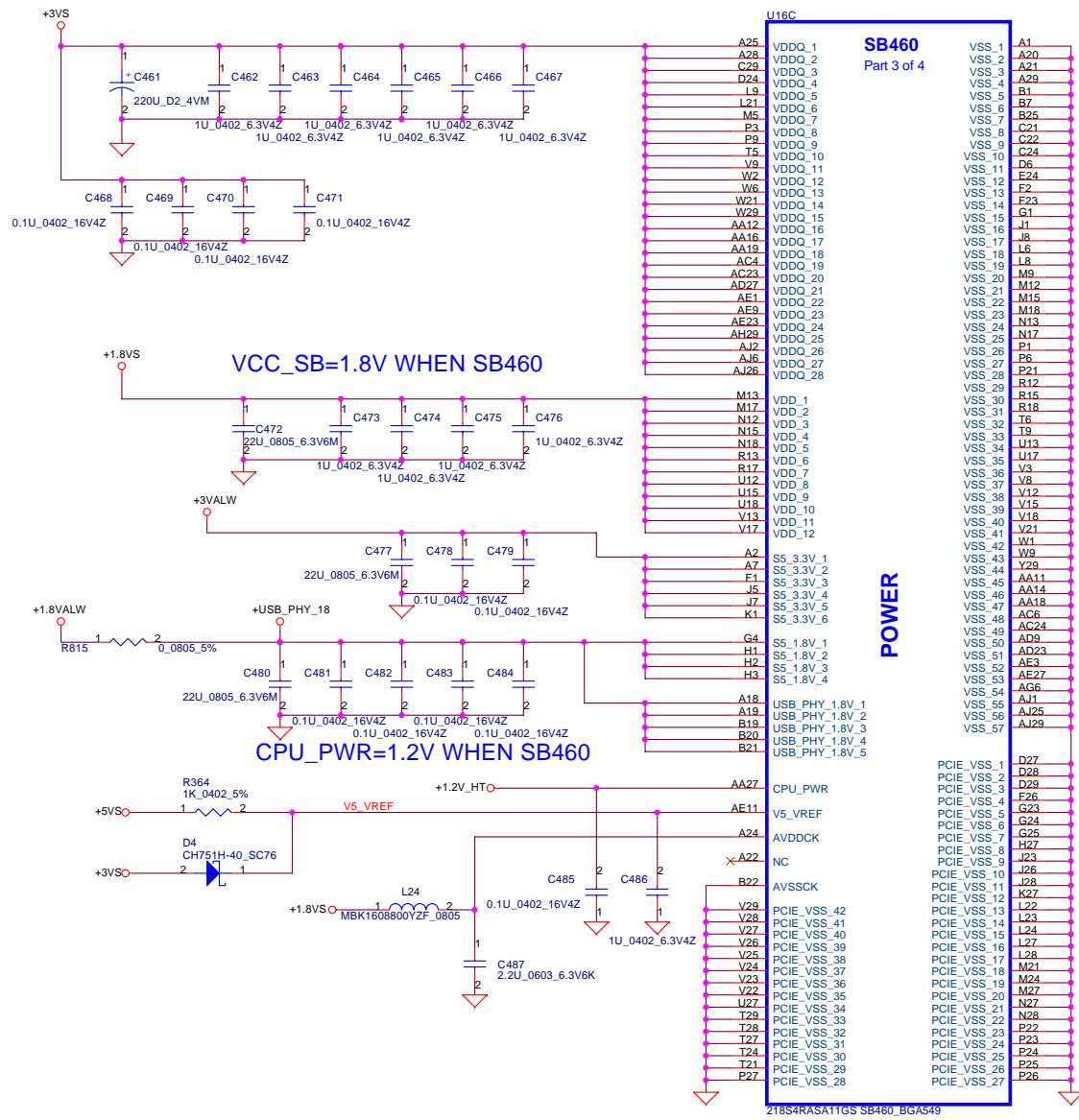
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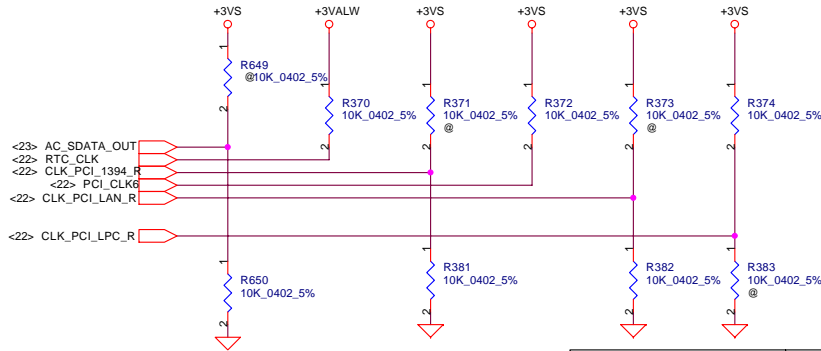
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REQUIRED STRAPS

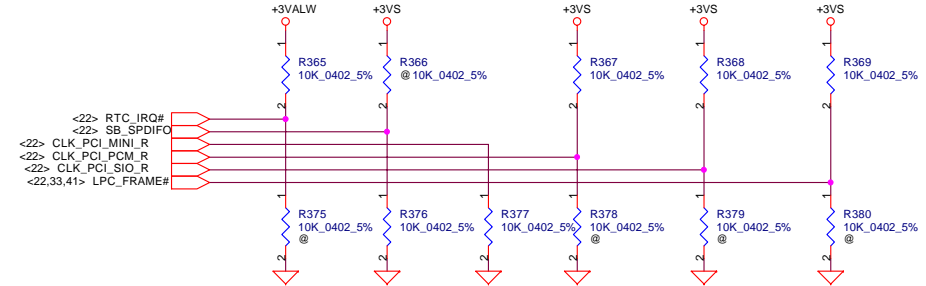
SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED



	SB600				SB460			
	AC_SDATA_OUT	RTC_CLK	PCI_CLK4 CLK_PCI_1394	PCI_CLK6	PCI_CLK0 CLK_PCI_LAN	PCI_CLK1 CLK_PCI_LPC	PCI_CLK0 CLK_PCI_LAN	PCI_CLK1 CLK_PCI_LPC
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	NOTE: FOR SB460, PCI_CLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCI_CLK[1:0]			

NOTE: R365 PU RESISTOR FOR
RTC_IRQ# IS REQUIRED FOR SB460
TO KEEP THE INPUT FROM FLOATING.

SB460 ONLY



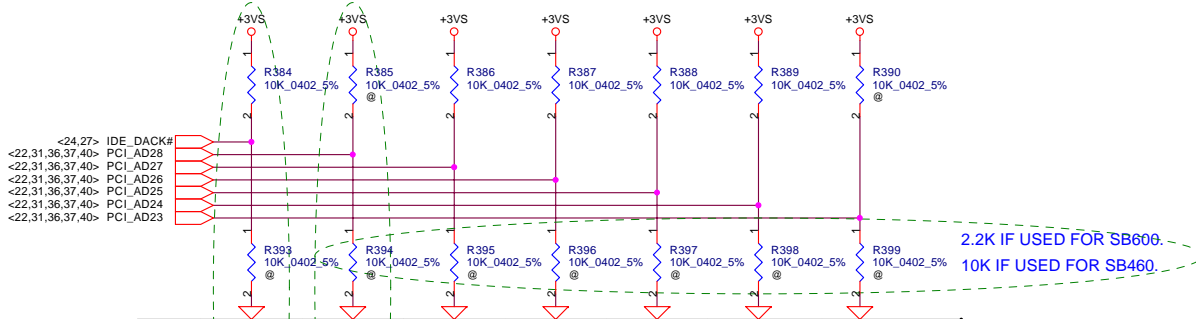
	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
	RTC_IRQ#	SB_SPDIFO	CLK_PCI_MINI	CLK_PCI_PCM	CLK_PCI_SIO	LPC_FRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHZ	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHZ DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#



OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB600 ONLY

NOTE: FOR
SB460,
PCI_AD23 IS
RESERVED

SB460 ONLY

SB600 ONLY

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Size	Document Number	Rev		Date	
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Sheet		26		of 55	

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<24> IDE_A[0..2] IDE_A[0..2]

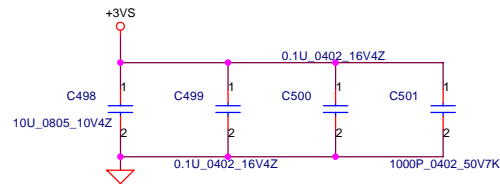
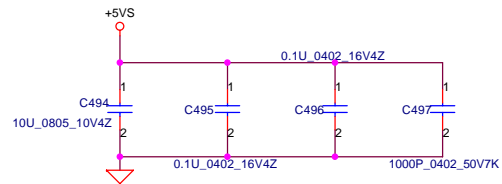
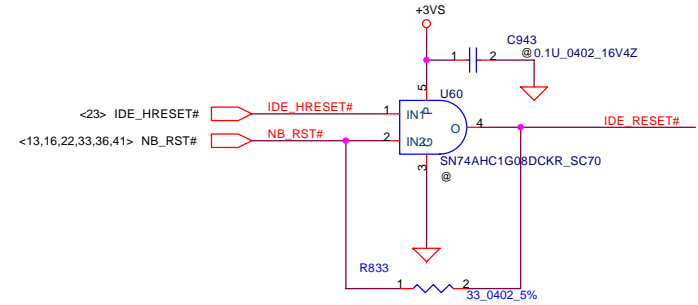


Diagram illustrating the SATA connector pinout for the OTEK SAT-22SG16 (NEW) SATA controller. The connector is labeled JP7 and has 22 pins.

Pin Connections:

- Pin 1: SATA_STX_C_DRX_P0
- Pin 2: SATA_STX_C_DRX_N0
- Pin 3: SATA_STX_C_DRX_P0
- Pin 4: SATA_STX_C_DRX_N0
- Pin 5: SATA_DTX_C_SRX_N0
- Pin 6: SATA_DTX_C_SRX_P0
- Pin 7: HRX-/HRX+
- Pin 8: +3VS
- Pin 9: VCC3.3
- Pin 10: VCC3.3
- Pin 11: GND
- Pin 12: GND
- Pin 13: GND
- Pin 14: VCC5
- Pin 15: VCC5
- Pin 16: VCC5
- Pin 17: GND
- Pin 18: RESERVED
- Pin 19: GND
- Pin 20: VCC12
- Pin 21: VCC12
- Pin 22: VCC12

Additional Information:

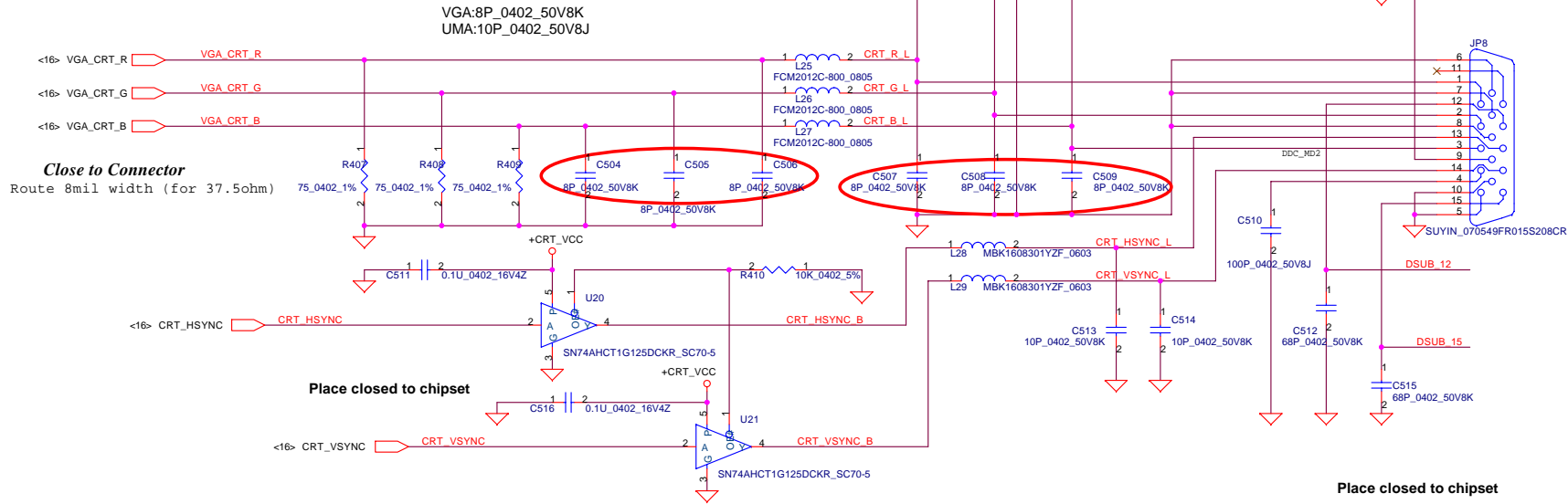
- Resistors R816 and R817 are shown in series with the +3VS and +5VS lines, respectively.
- Termination resistors are indicated by zigzag symbols on the +3VS and +5VS lines.
- Values 0.0805_5% are noted for the termination resistors.
- A note at the bottom left states: "Modify 11/07 for EMI".
- The bottom right corner identifies the component as "SATA@ OTEK_SAT-22SG16 (NEW)".

Pin-to-pin connection diagram for the J16 connector. The diagram shows connections between IDE signals (RESET#, D7-D0, D15-D0, IOW#, IORDY, IRQ, A1-A0, CS1#, LED#) and IDE D signals (D8-D0, DREQ, IOR#). It also shows connections for +5V, SD_CSEL, SATA, and OCTEC_CDR-50J1LG. Components like resistors R783, R405, R782, and R406 are shown with values like 470_0402_5% and 100K_0402_5%. A 80mils dimension is indicated for the SD_CSEL connection.

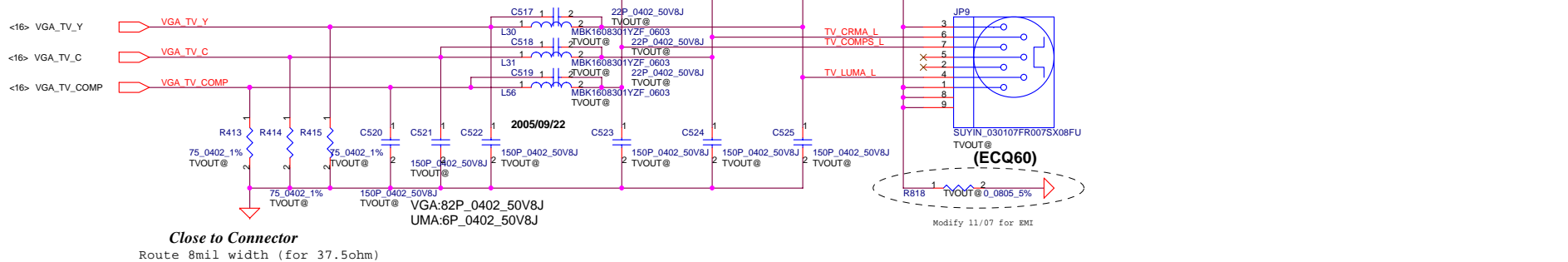
Compal Electronics, Inc.			
Title			
SCHEMATIC, M/B LA-3151P			
Size	Document Number		Rev
	401412		B
Date:	星期四, 三月 09, 2006		Sheet 27 of 55

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CRT Connector



TV-OUT Conn.



Close to Connector

Route 8mil width (for 37.5ohm)

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LCD POWER CIRCUIT

07/07/'05

+LCDVDD

+5VALW

R416 360_0402_5%

R417 100K_0402_5%

R418 1K_0402_5%

Q9 2N7002_SOT23

C526 0.047U_0402_16V4Z

+3VS

W=60mils

Q10 SI2301BDS_SOT23

W=60mils

+LCDVDD

C893 4.7U_0805_10V4Z

C894 0.1U_0402_16V4Z

<17> ENVDD

ENVD

R419 10K_0402_5%

Q11 BSS138_SOT23

+3VS

C529 0.1U_0402_16V4Z

D15 @1N4148_SOT23

INVT_PWM

C530 @1U_0402_6.3V4Z

<33> BKOFF#

BKOFF#

D14 RB751V_SOD323

R420 4.7K_0402_5%

DISPOFF#

+INVPWR_B+

L45 KC FBM-LT1-201209-221LMAT_0805

L46 KC FBM-LT1-201209-221LMAT_0805

C790 68P_0402_50V8K

LCD/PANEL BD. Conn.

JP10

+INVPWR_B+

KC FBM-LT1-201209-221LMAT_0805

+3VS

L72

<16> I2C_CLK

I2C_CLK

<16> I2C_DAT

I2C_DAT

<17> VGA_LVDSB0-

VGA_LVDSB0+

TZOUT0-

TZOUT0+

<17> VGA_LVDSB1-

VGA_LVDSB1+

TZOUT1-

TZOUT1+

<17> VGA_LVDSB2-

VGA_LVDSB2+

TZOUT2-

TZOUT2+

<17> VGA_LVDSBC-

VGA_LVDSBC+

TZCLK-

TZCLK+

(60 MIL)

KC FBM-LT1-201209-221LMAT_0805

L73

DAC_BRIG <33>

INVT_PWM <33>

DISPOFF#

+LCDVDD

VGA_LVDSA0-

VGA_LVDSA0+

VGA_LVDSA1-

VGA_LVDSA1+

VGA_LVDSA2-

VGA_LVDSA2+

VGA_LVDSAC-

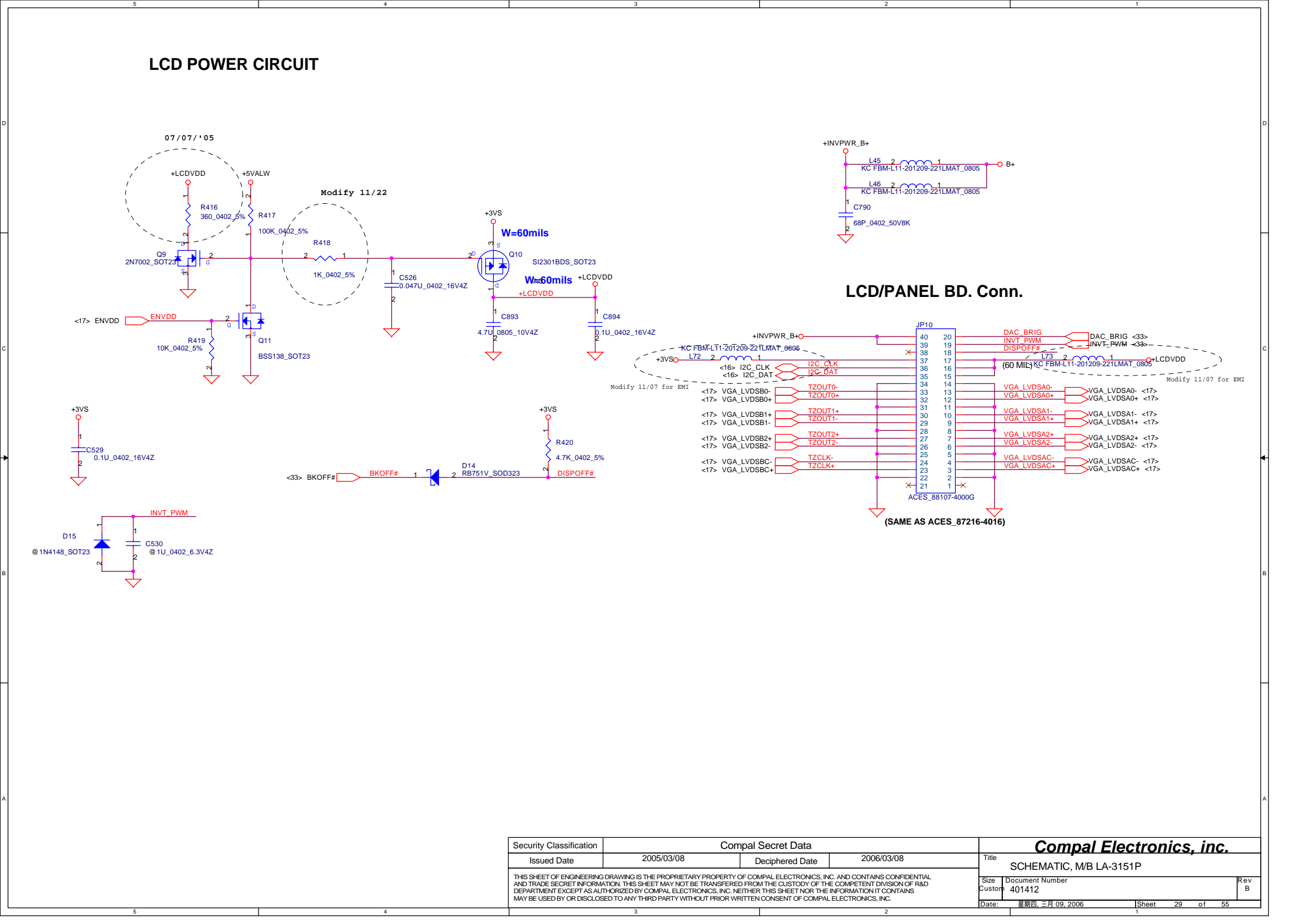
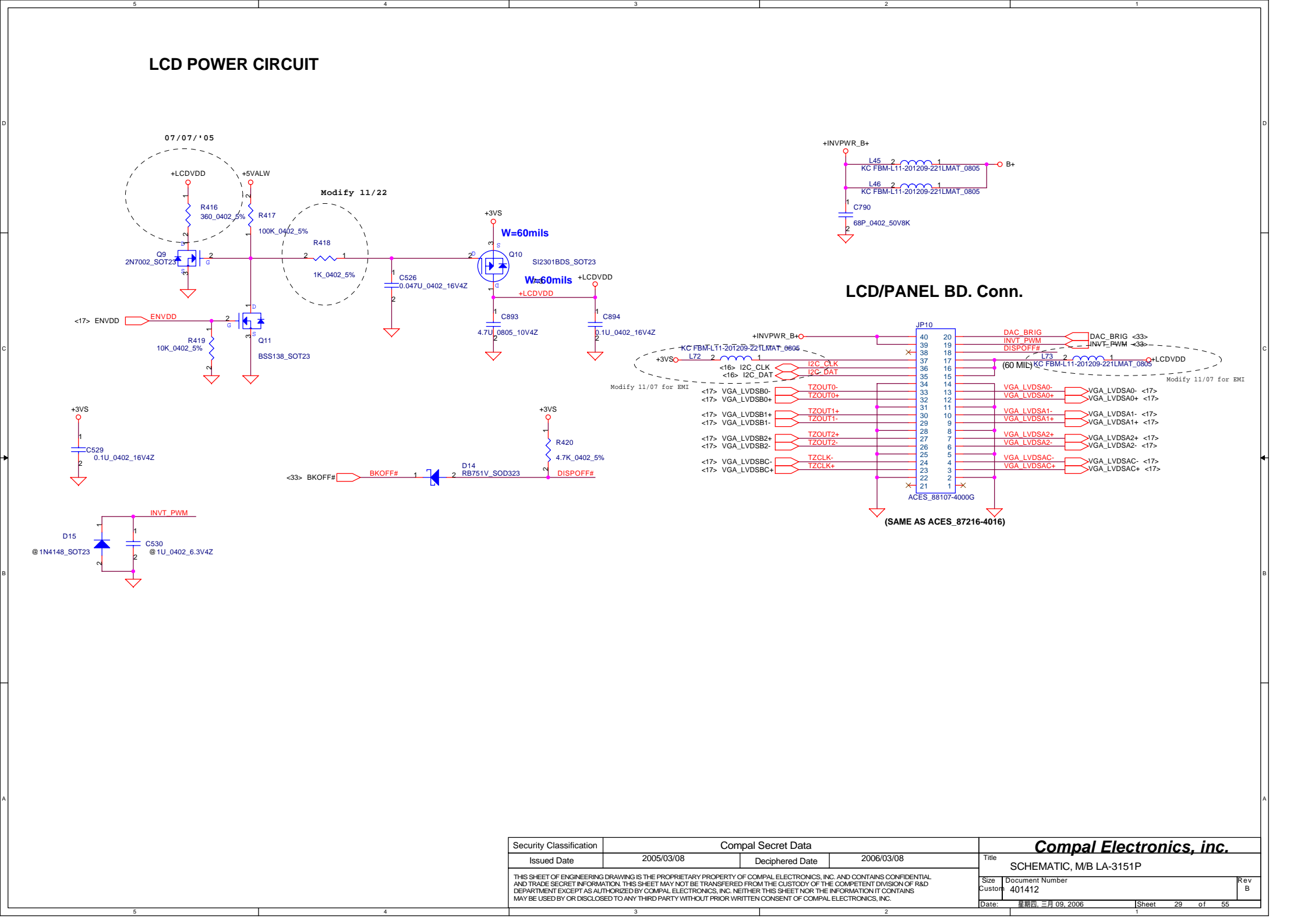
VGA_LVDSAC+

Modify 11/07 for EMI

ACES_88107-4000G

(SAME AS ACES_87216-4016)

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This figure is a detailed schematic diagram of the LCD Power Circuit and LCD/PANEL Board Connection for a device, likely a mobile phone or PDA, as indicated by the part number 401412.

LCD POWER CIRCUIT:

- Power Input:** +3VS (3.3V) and +5VALW (5V) are the main power inputs.
- Regulation:** The +5VALW input is regulated by a 360k resistor (R416) and a 100k resistor (R417) to provide +LCDVDD. The +3VS input is regulated by a 4.7k resistor (R420) to provide +LCDVDD.
- Switching:** The +5VALW input is controlled by a MOSFET (Q9, 2N7002) and a MOSFET (Q10, SI2301BDS). The +3VS input is controlled by a MOSFET (Q11, BSS138).
- Capacitors:** Various capacitors are used for decoupling and filtering, including 0.047uF (C526), 0.1uF (C529, C894), 0.047uF (C893), 0.1uF (C530), and 0.047uF (C526).
- Diodes:** A diode (D15, 1N4148) is used for protection.
- Control:** The circuit is controlled by signals like ENVDD, BKOFF#, and INVT_PWM.

LCD/PANEL BD. Conn.:

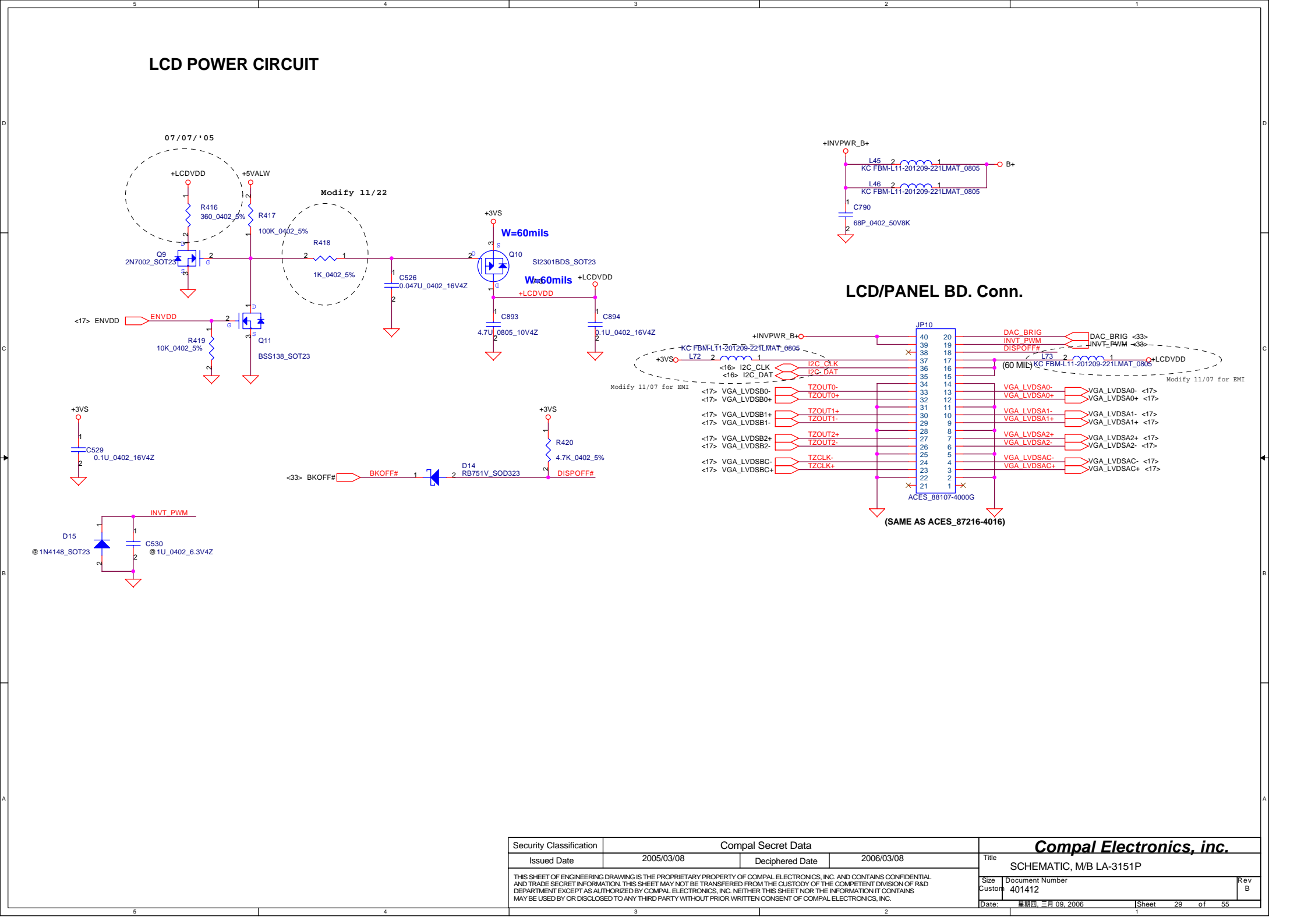
- Connector:** The connection is made via a 40-pin connector (JP10).
- Signals:** The signals include DAC_BRIG, INVT_PWM, DISPOFF#, I2C_CLK, I2C_DAT, TZOUT0+, TZOUT1+, TZOUT2+, TZCLK+, TZCLK-, and various LVDS signals (VGA_LVDSA0+, VGA_LVDSA0-, VGA_LVDSA1+, VGA_LVDSA1-, VGA_LVDSA2+, VGA_LVDSA2-, VGA_LVDSA3+, VGA_LVDSA3-).
- Termination:** The signals are terminated with 60 ohm resistors (L73, L74).

Legend:

- W=60mils: Width of the traces.
- W=60mils: Width of the traces.

Table:

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LCD POWER CIRCUIT

07/07/'05

Modify 11/22

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W=60mils

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W=60mils

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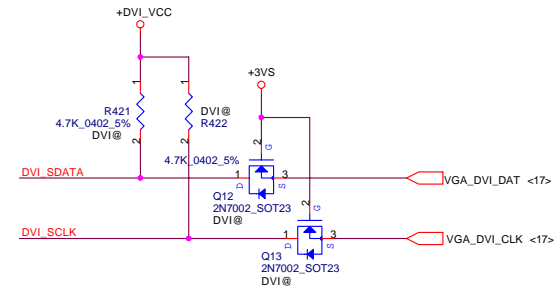
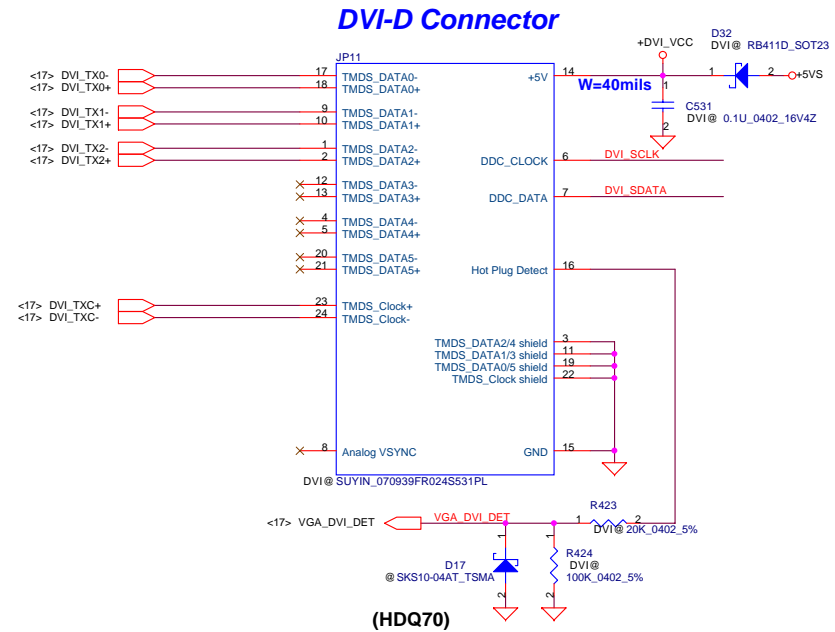
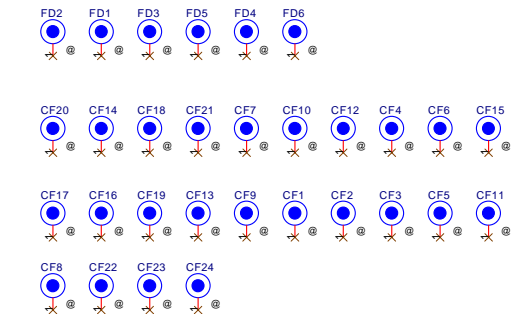
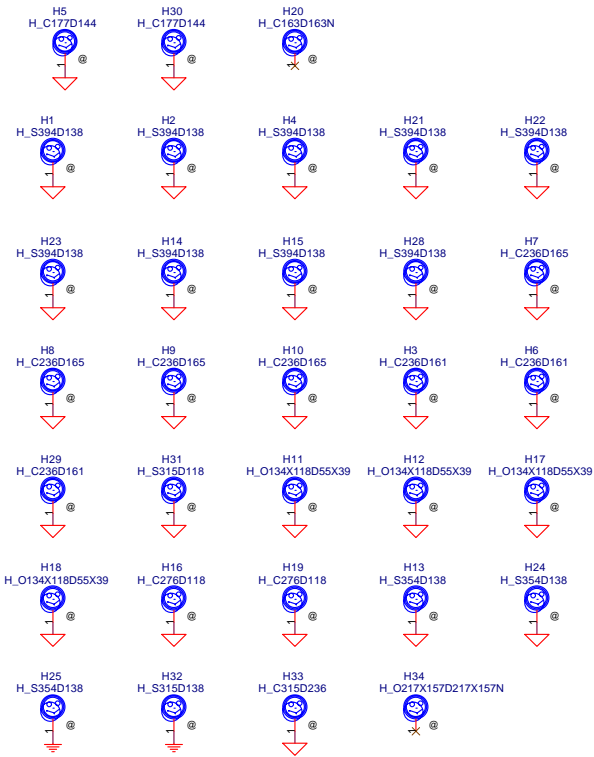
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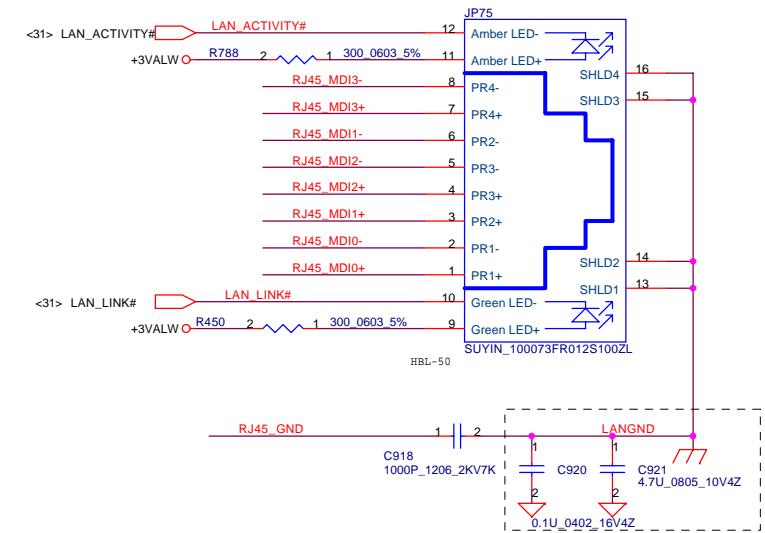
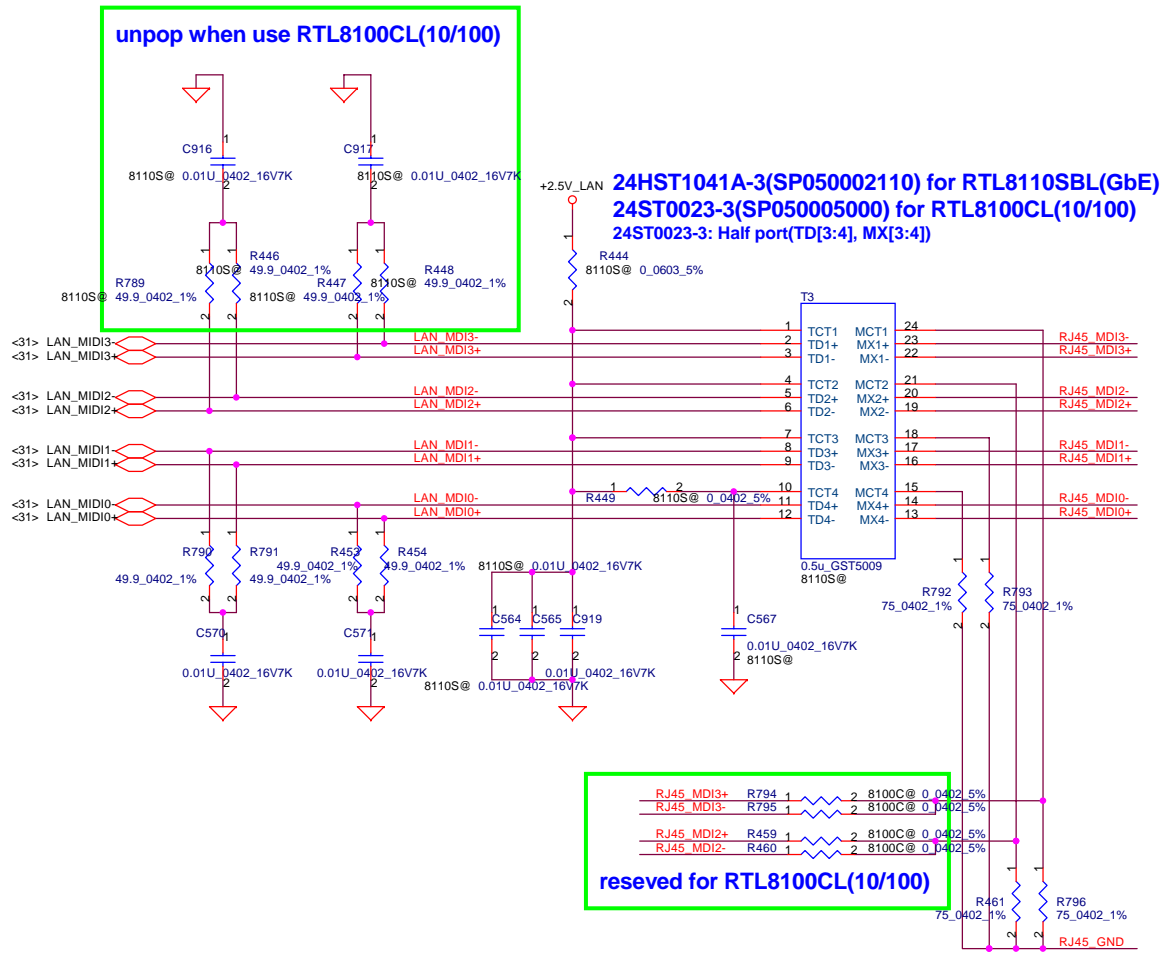
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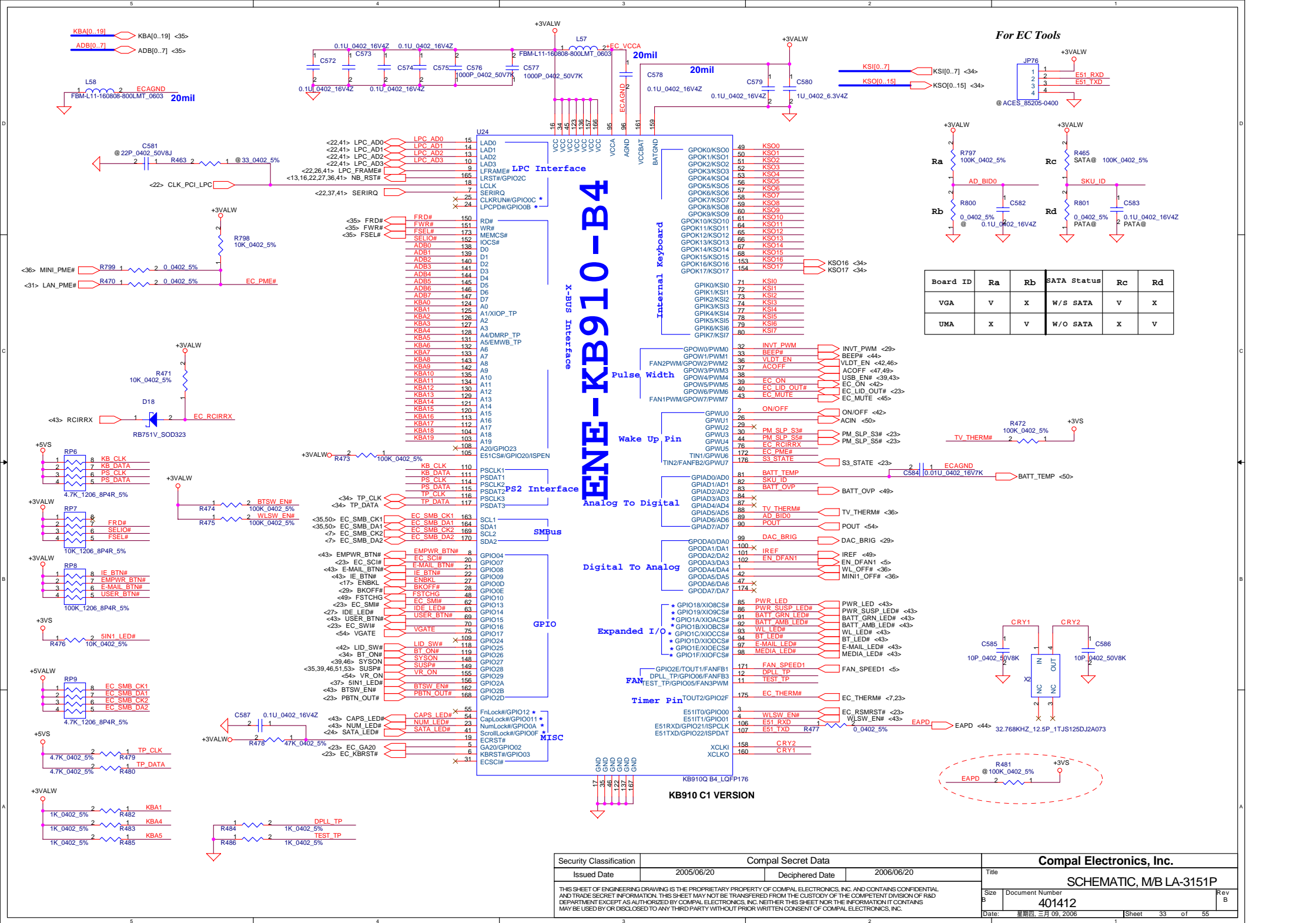


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								Size B	Document Number						Rev B	
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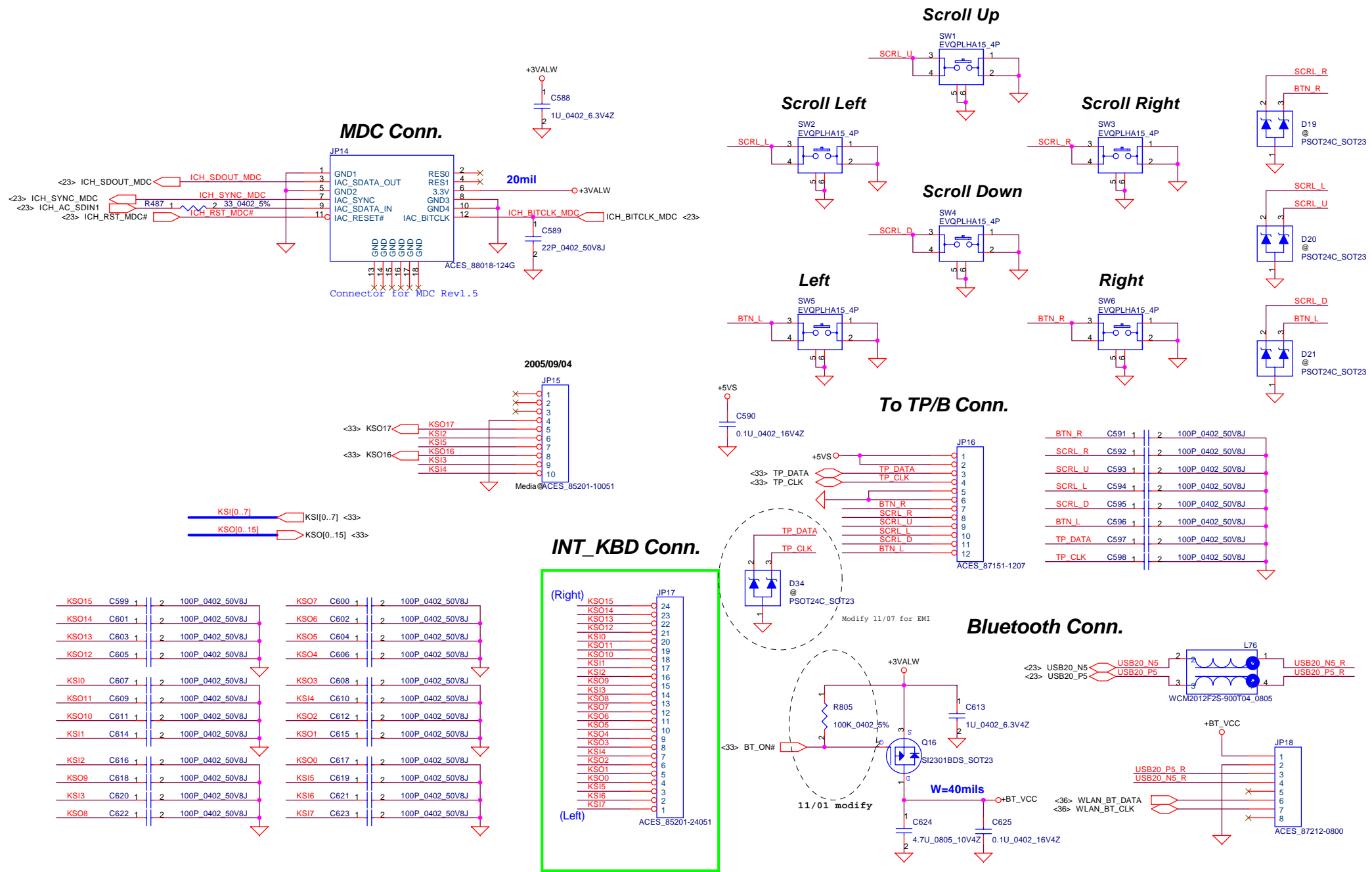
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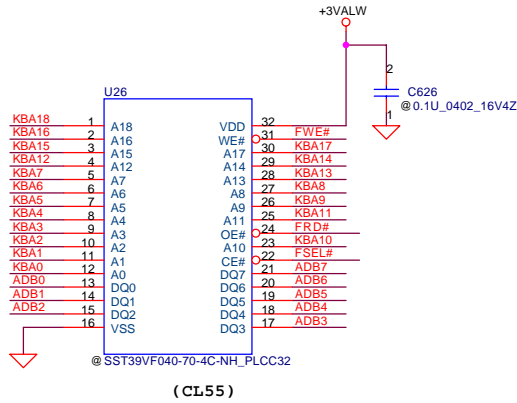


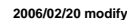
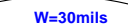
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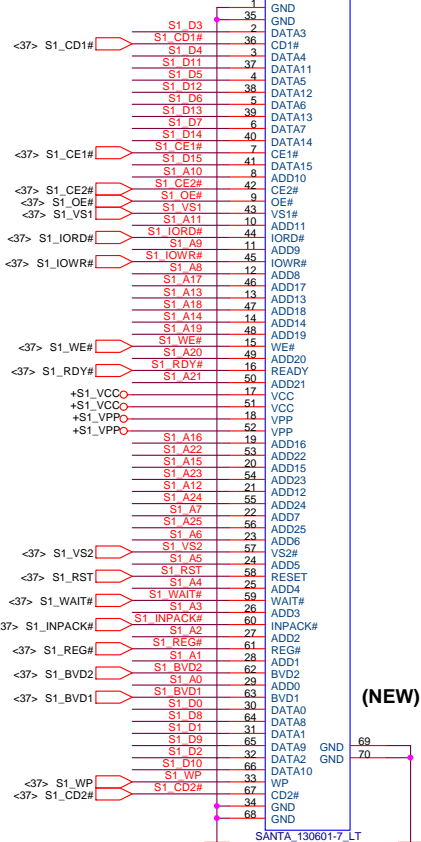
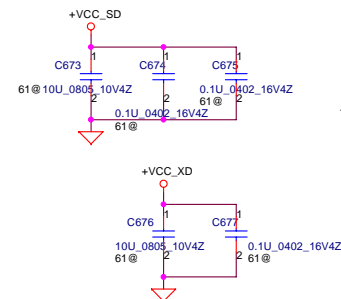
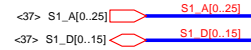
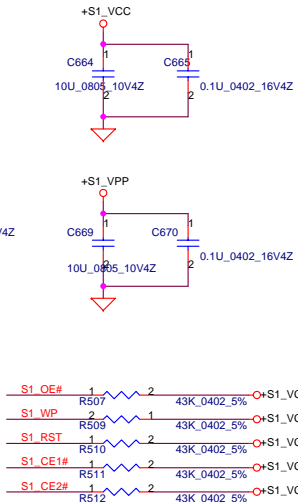
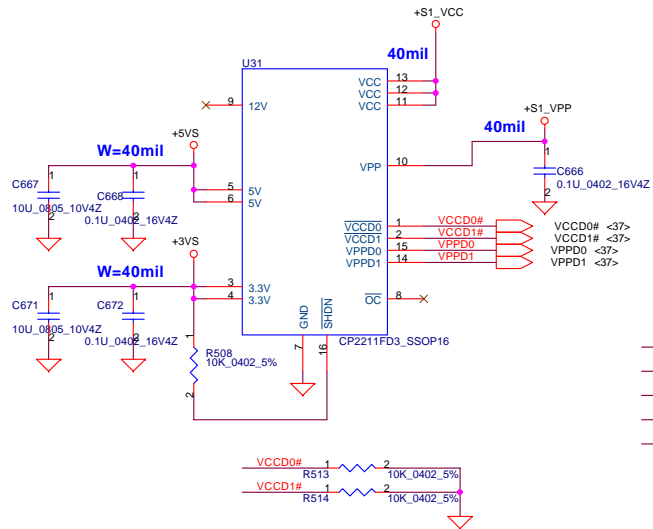
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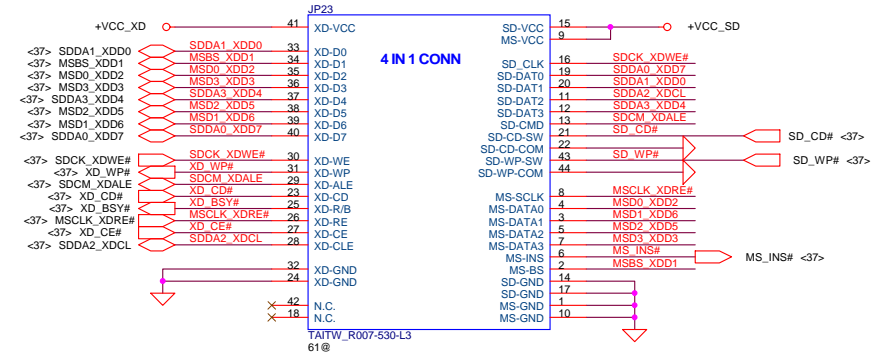
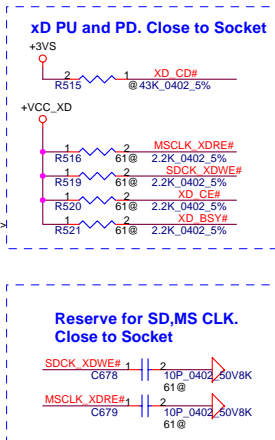
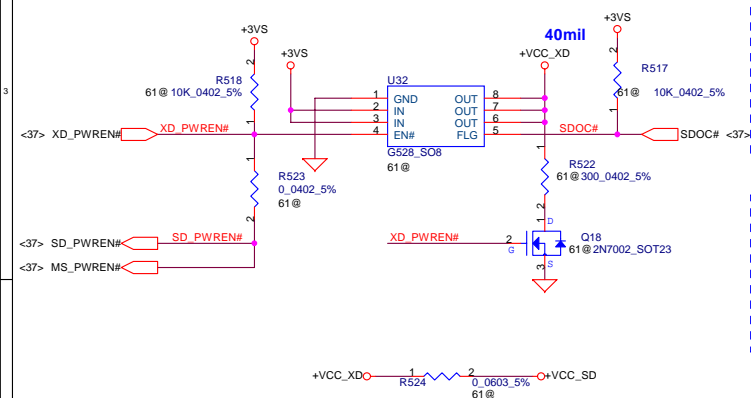


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PCMCIA Power Control



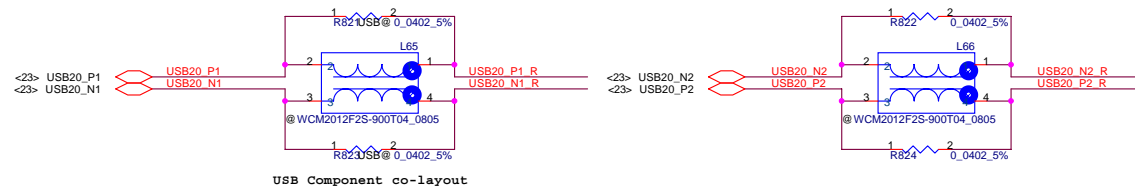
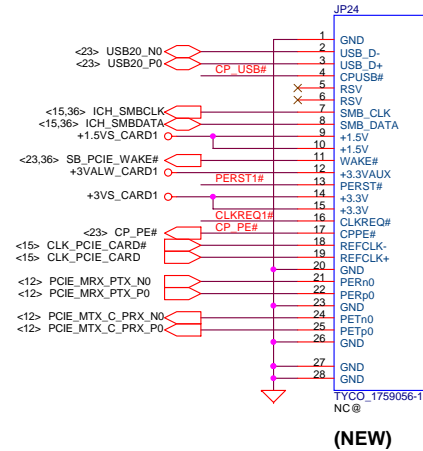
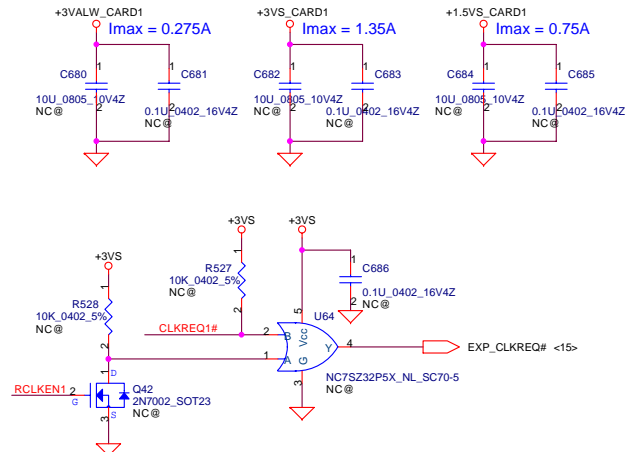
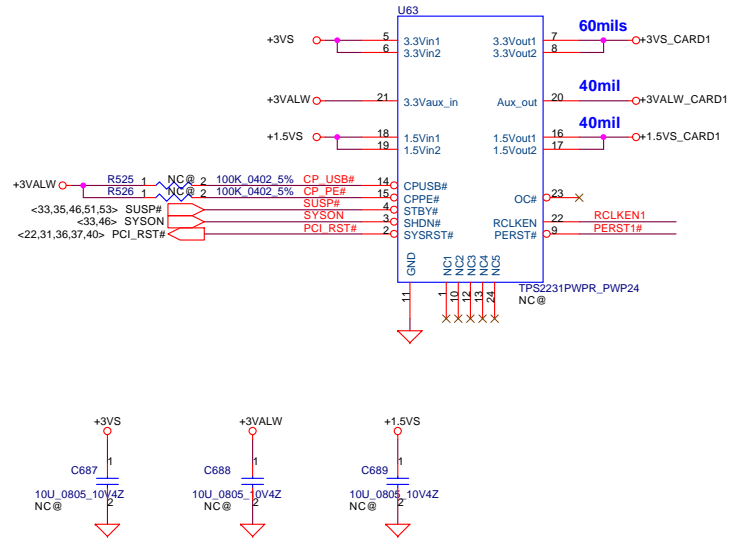
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XD Power Control



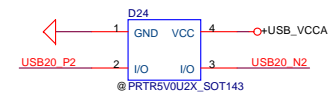
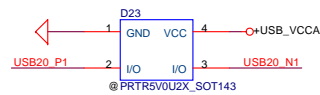
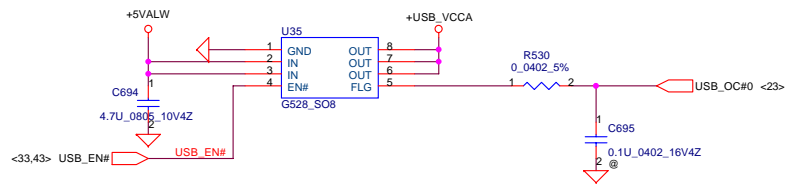
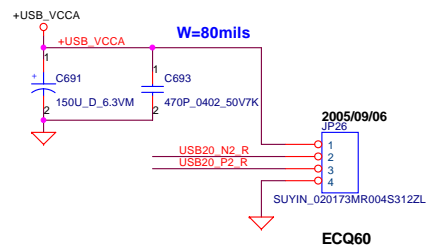
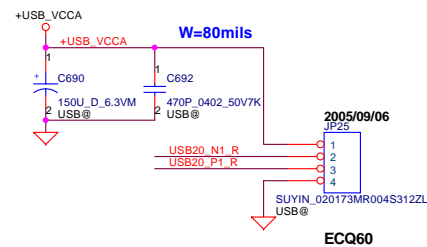
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New Card Power Switch

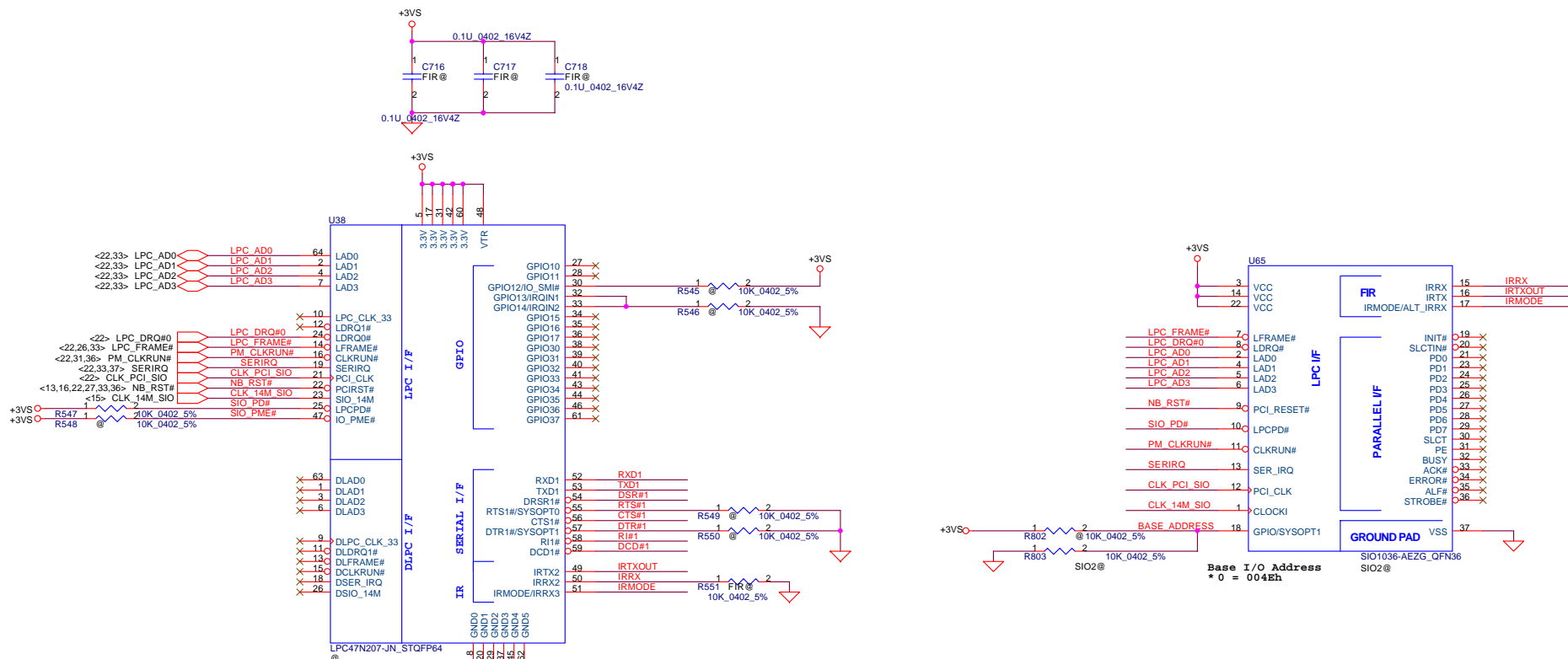


USB CONN. 1 & 2



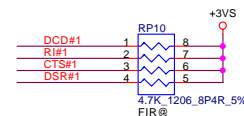
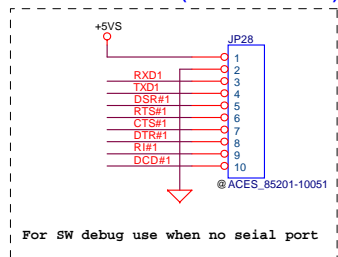
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SUPER I/O SMsC LPC47N207

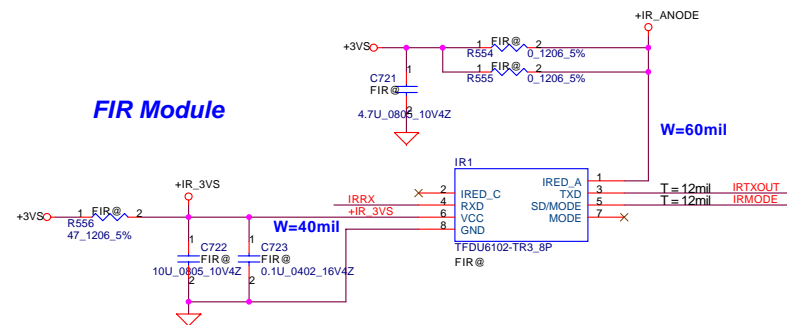


RTS#1
Base I/O Address
* 0 = 02Eh
1 = 04Eh

Place on the BOT side(near MINIPCI conn.)

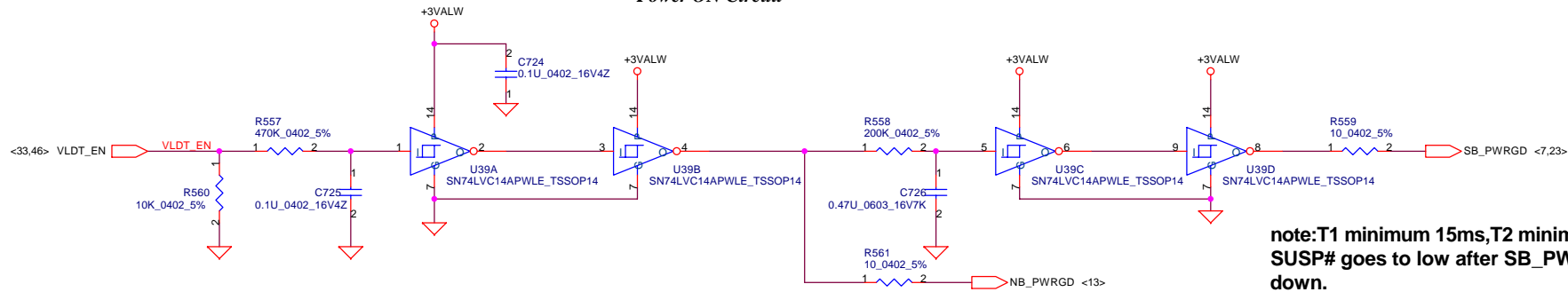


FIR Module

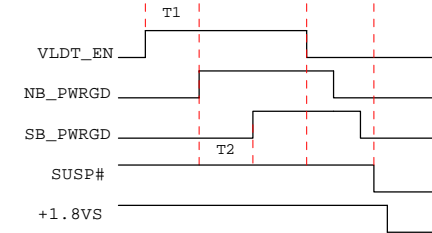


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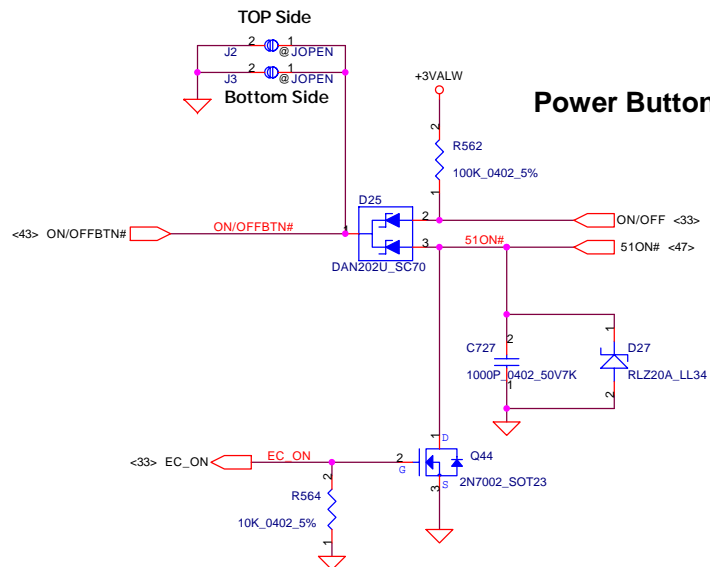
Power ON Circuit



note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,
SUSP# goes to low after SB_PWRGD goes to low for power
down.

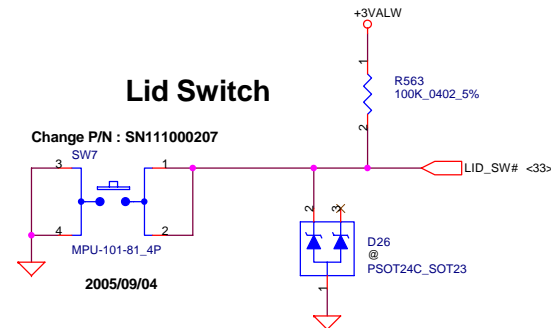


ON/OFF switch

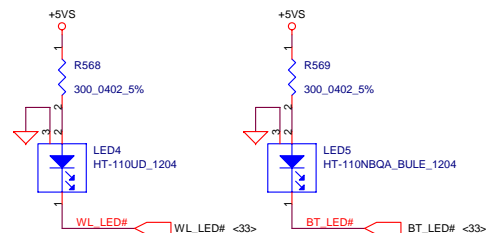
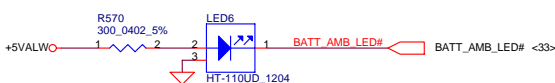
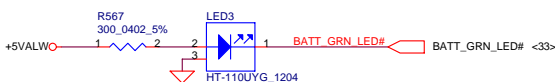
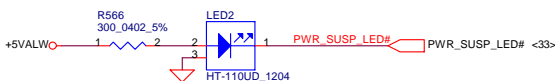
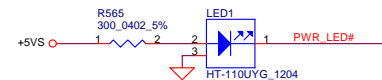
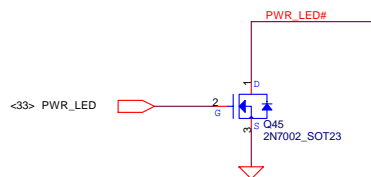


Power Button

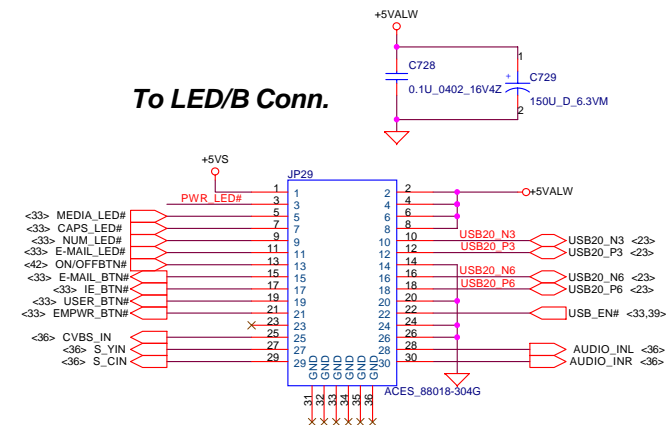
Lid Switch



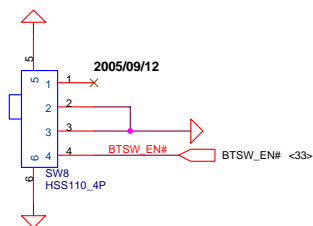
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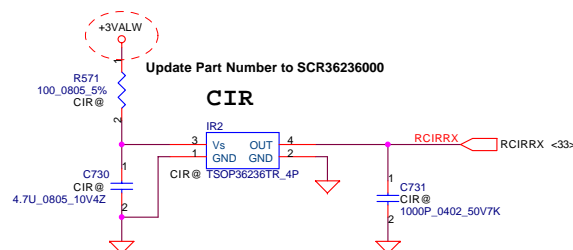
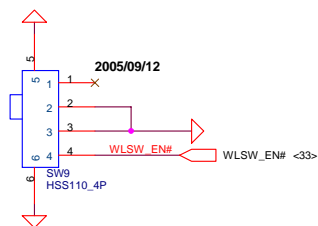
To LED/B Conn.



BT_SW

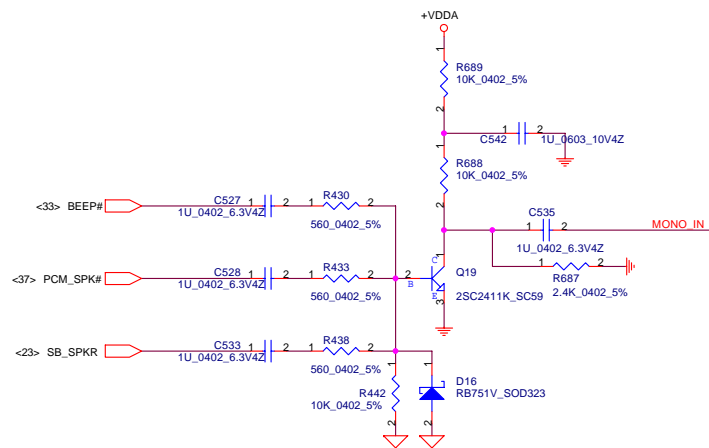


WL_SW

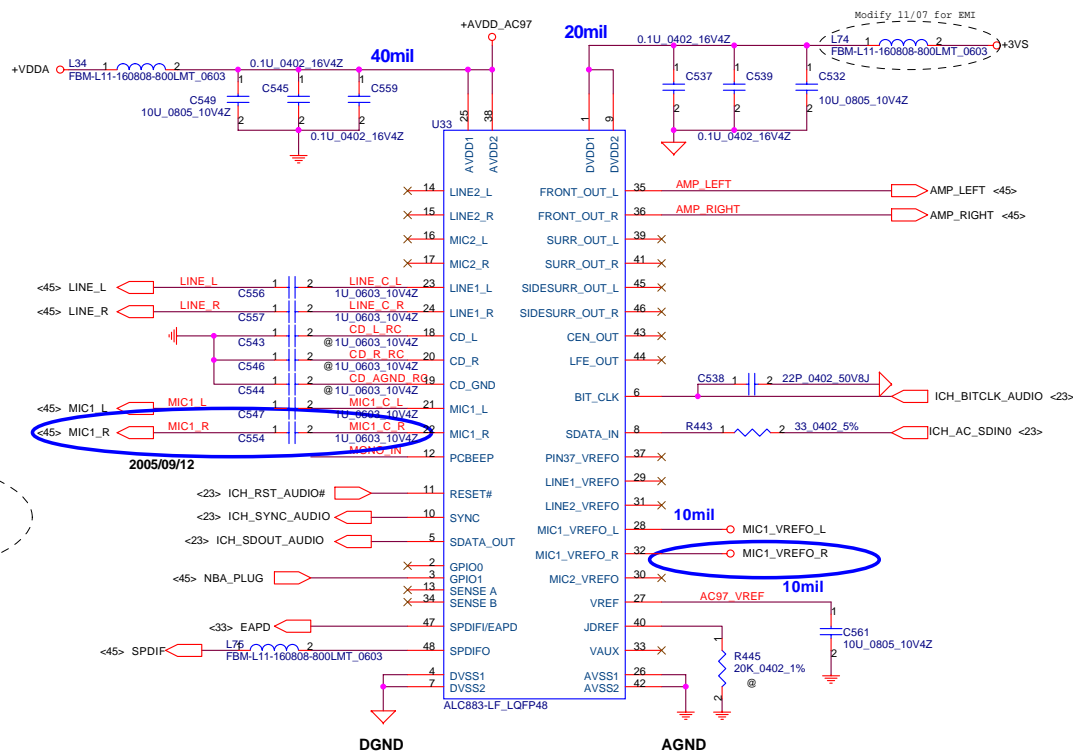


Geneva		Grapevine	
	KSO16	KSO17	
KSI0	VOL_UP	LEFT	
KSI1	RIGHT	VOL_DOWN	
KSI2	PLAY	ENTER	
KSI3	STOP		
KSI4	NEXT		
KSI5	REV		
KSI6		RECORD	

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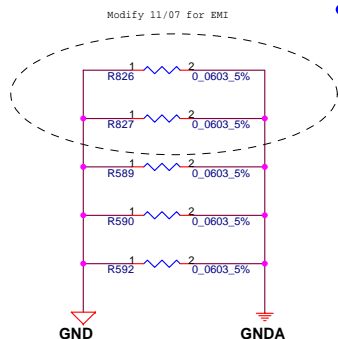


HD Audio Codec

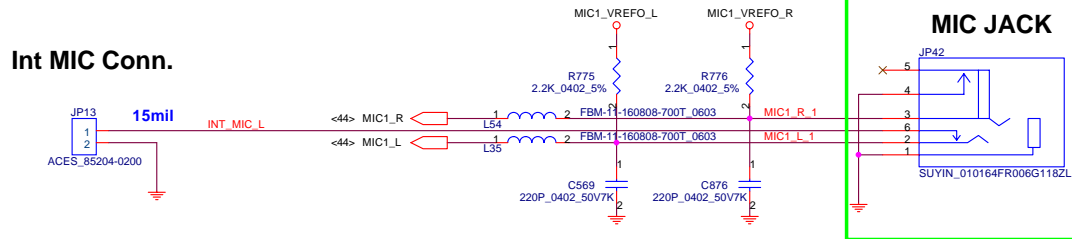
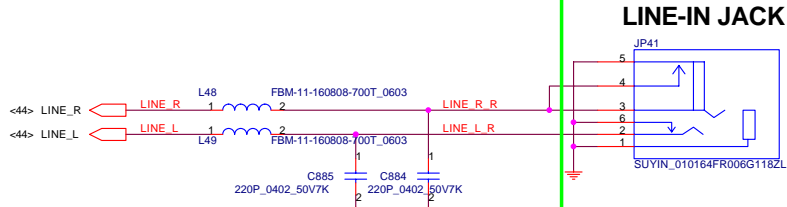
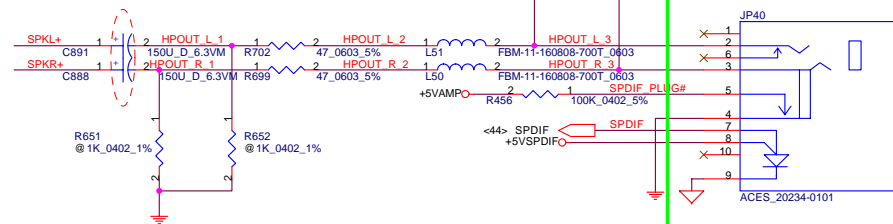
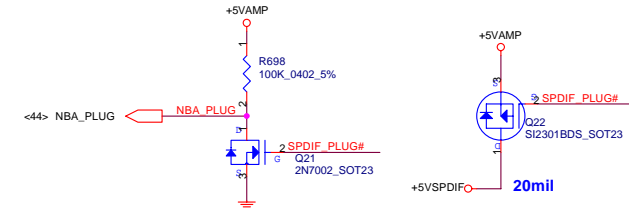
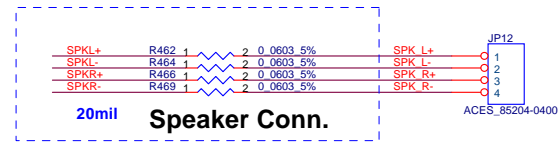
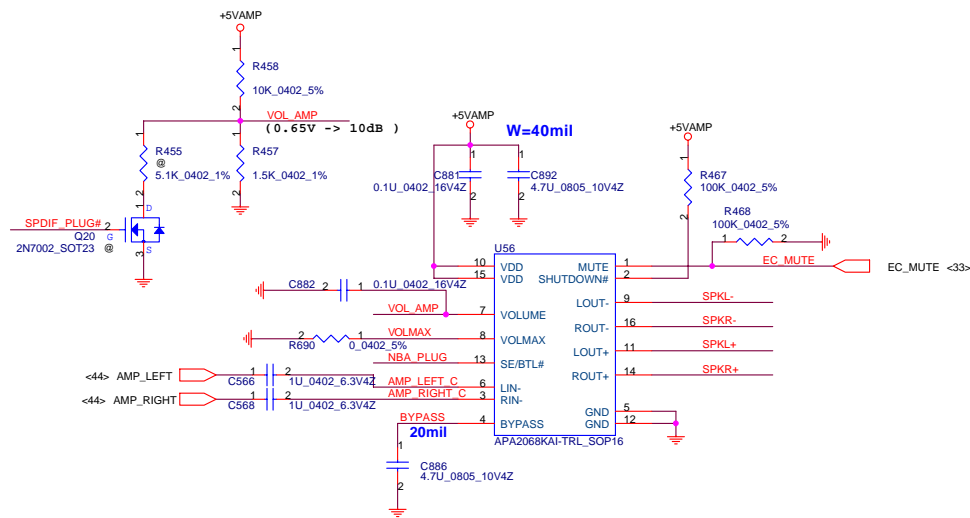


28.7K for Module Design (VDDA = 4.702)

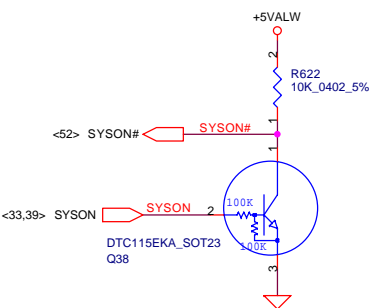
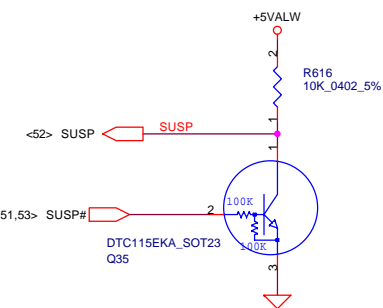
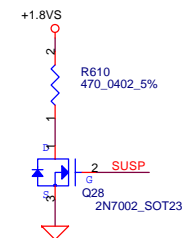
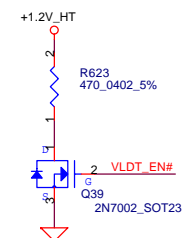
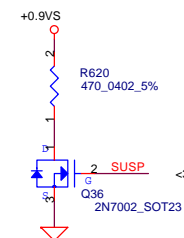
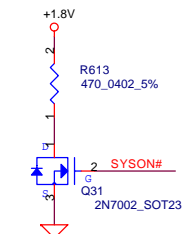
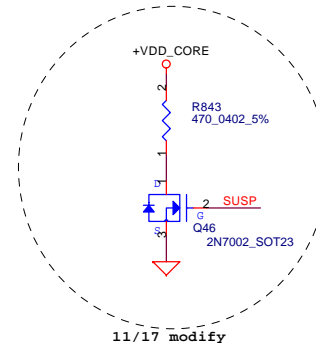
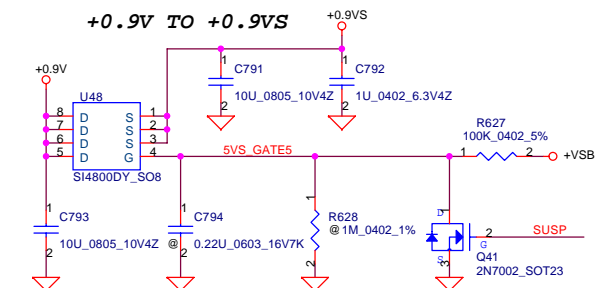
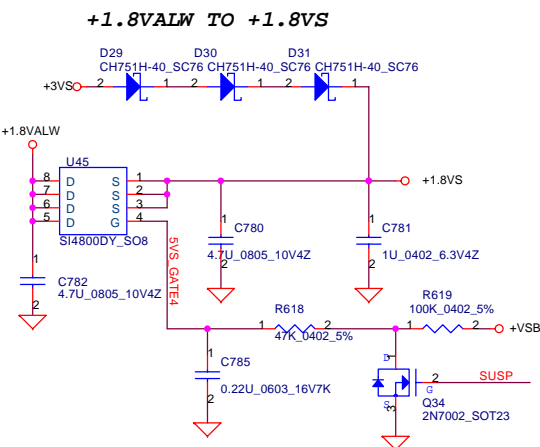
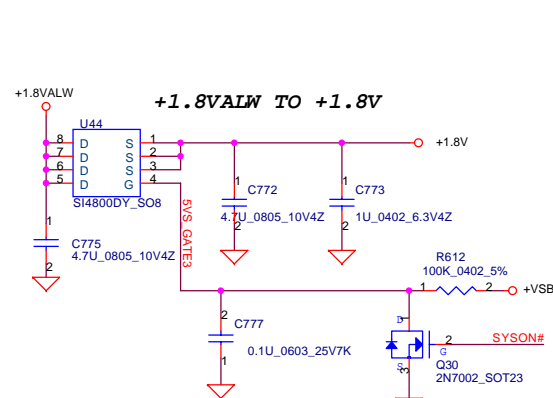
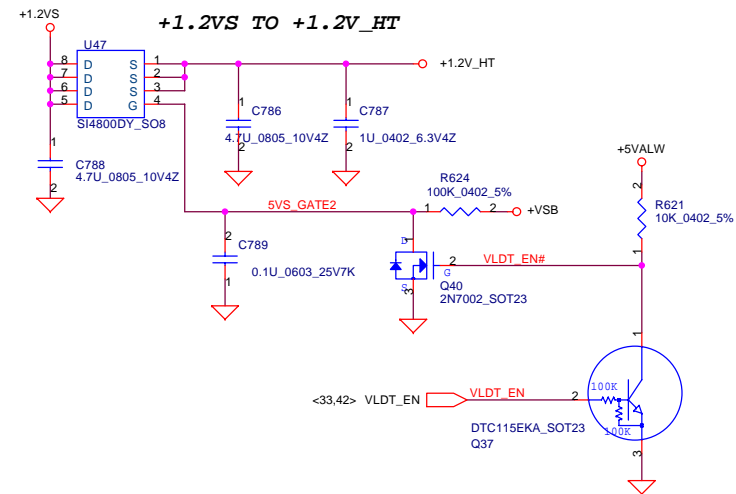
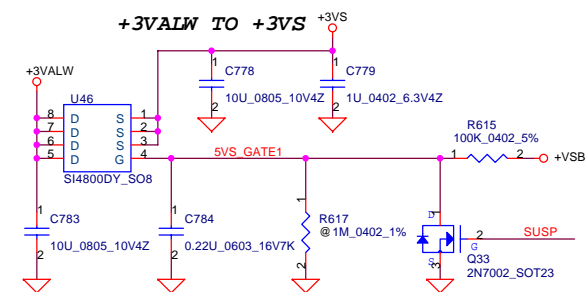
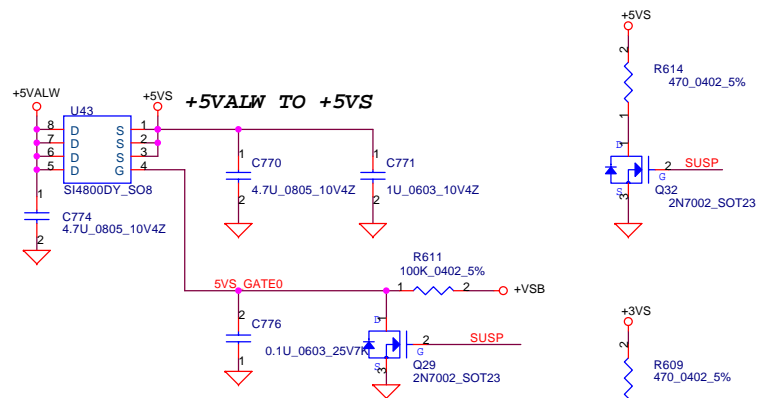
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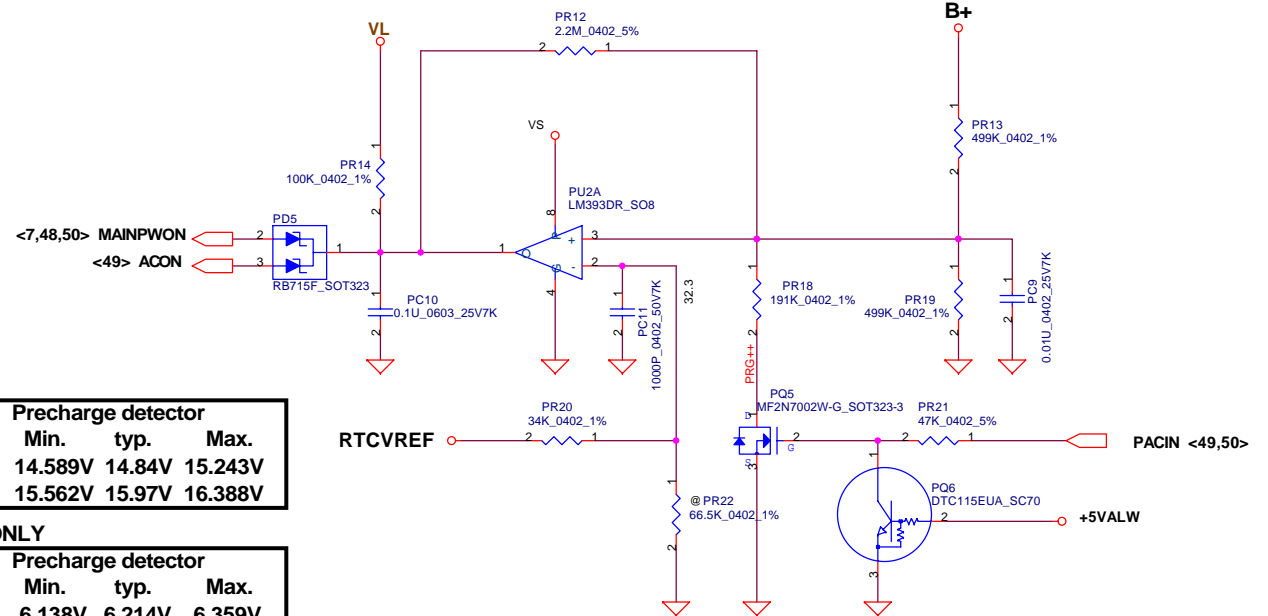
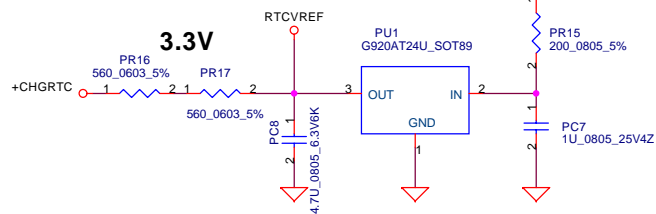
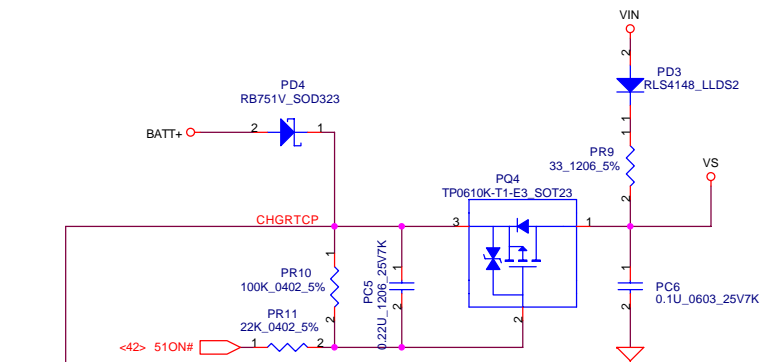
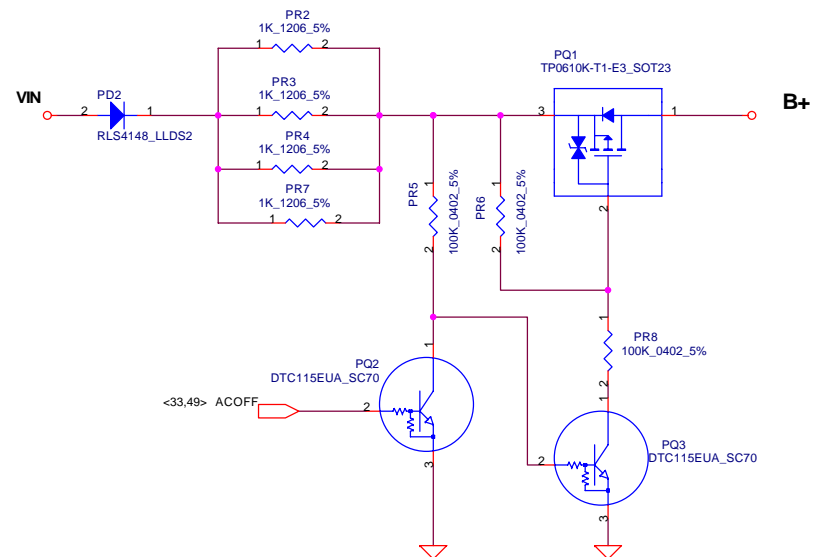
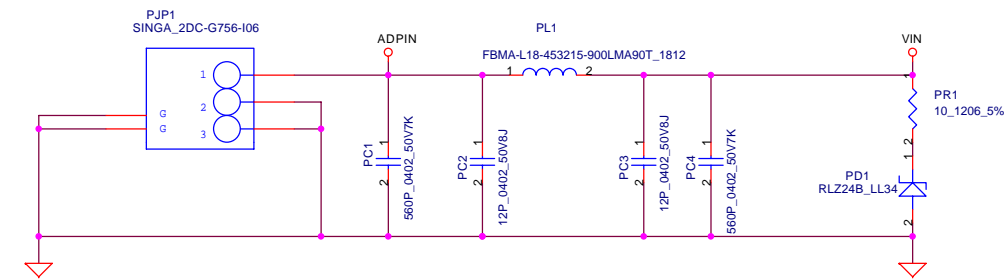
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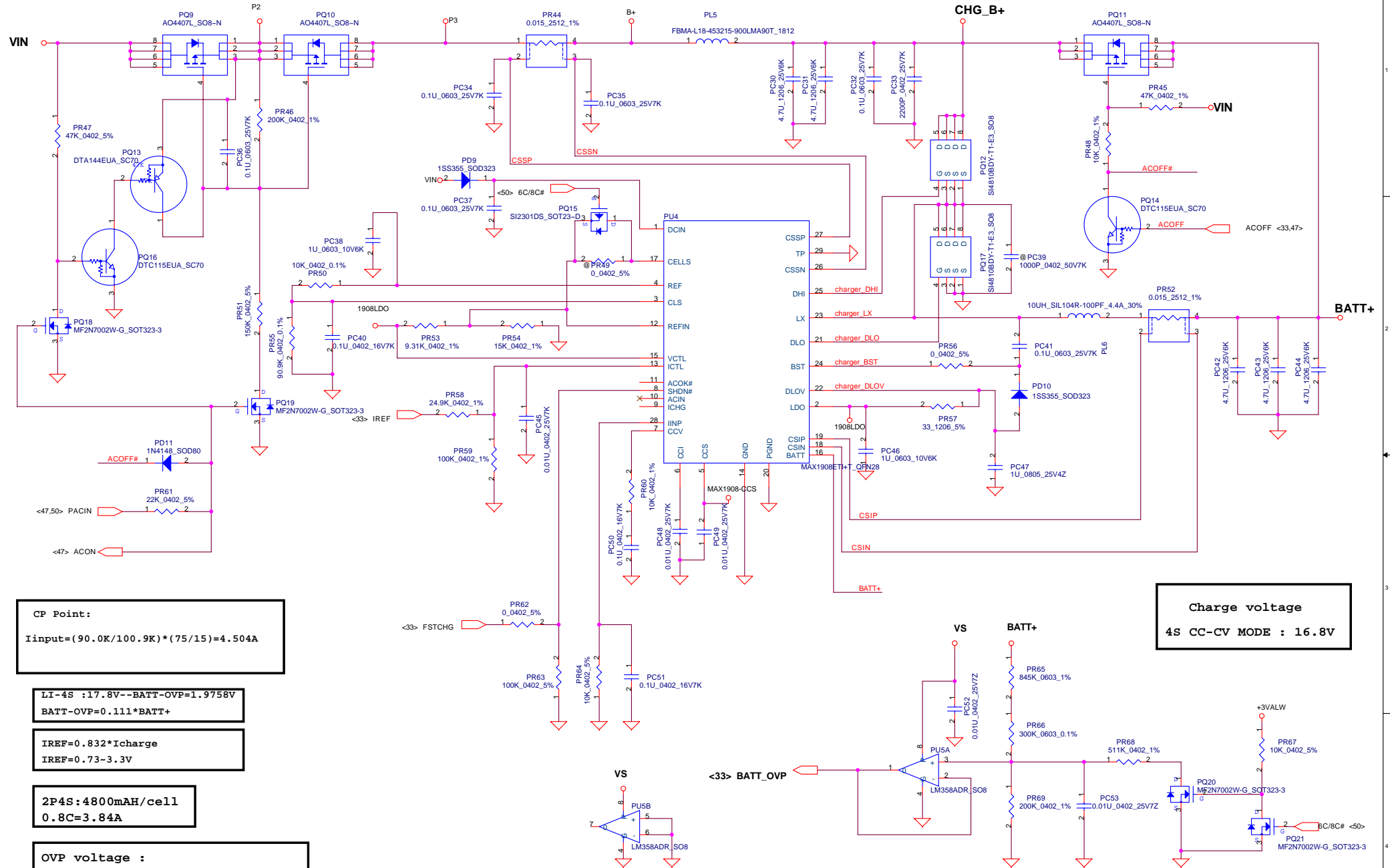
ACIN

	Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V	
L-->H	15.562V	15.97V	16.388V	

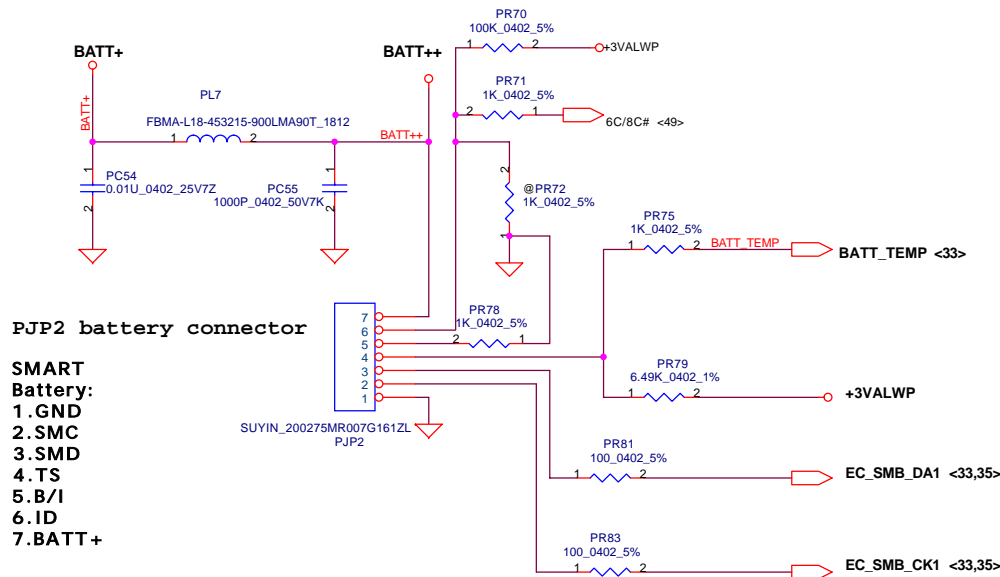
BATT ONLY

	Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V	
L-->H	7.196V	7.349V	7.505V	

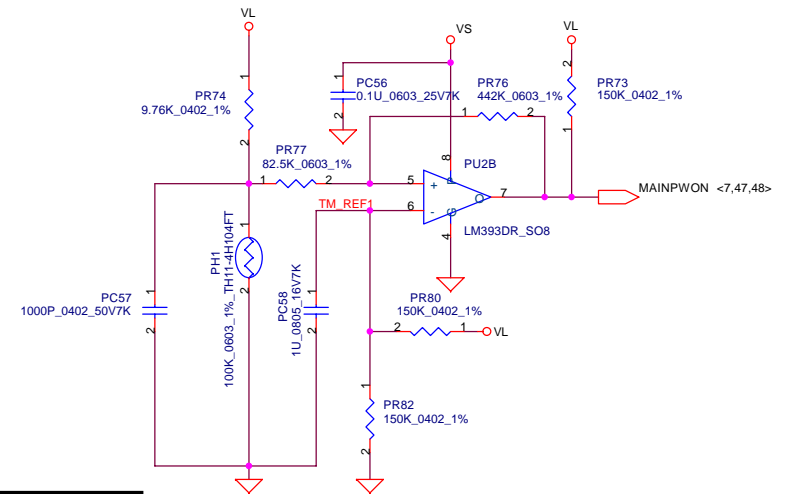
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I_{adp}=0~4.5A(90W)

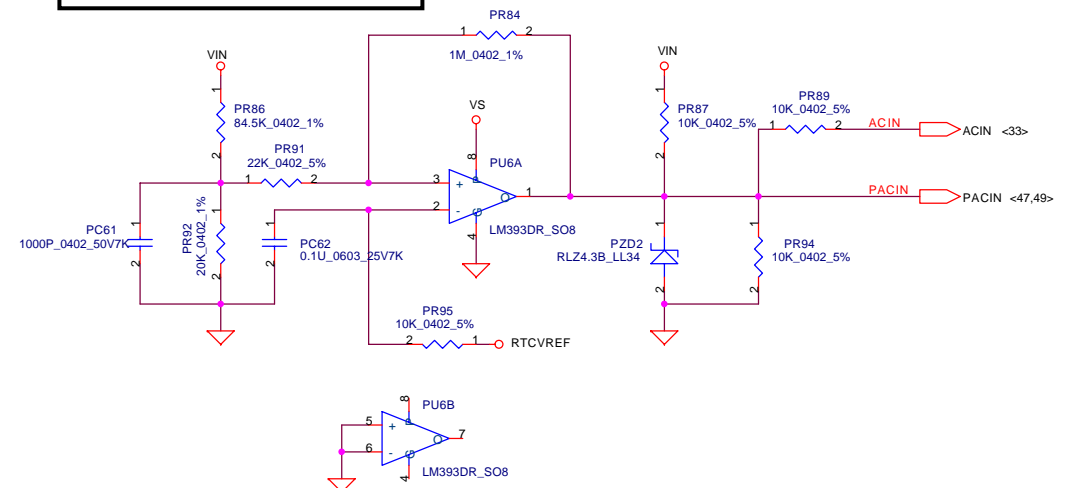
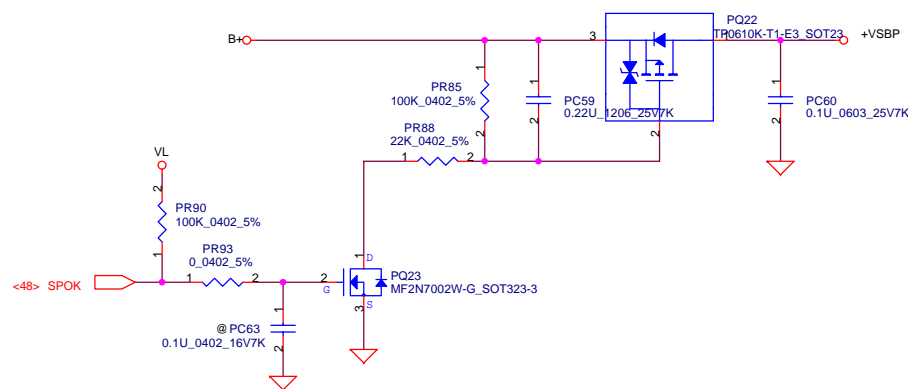
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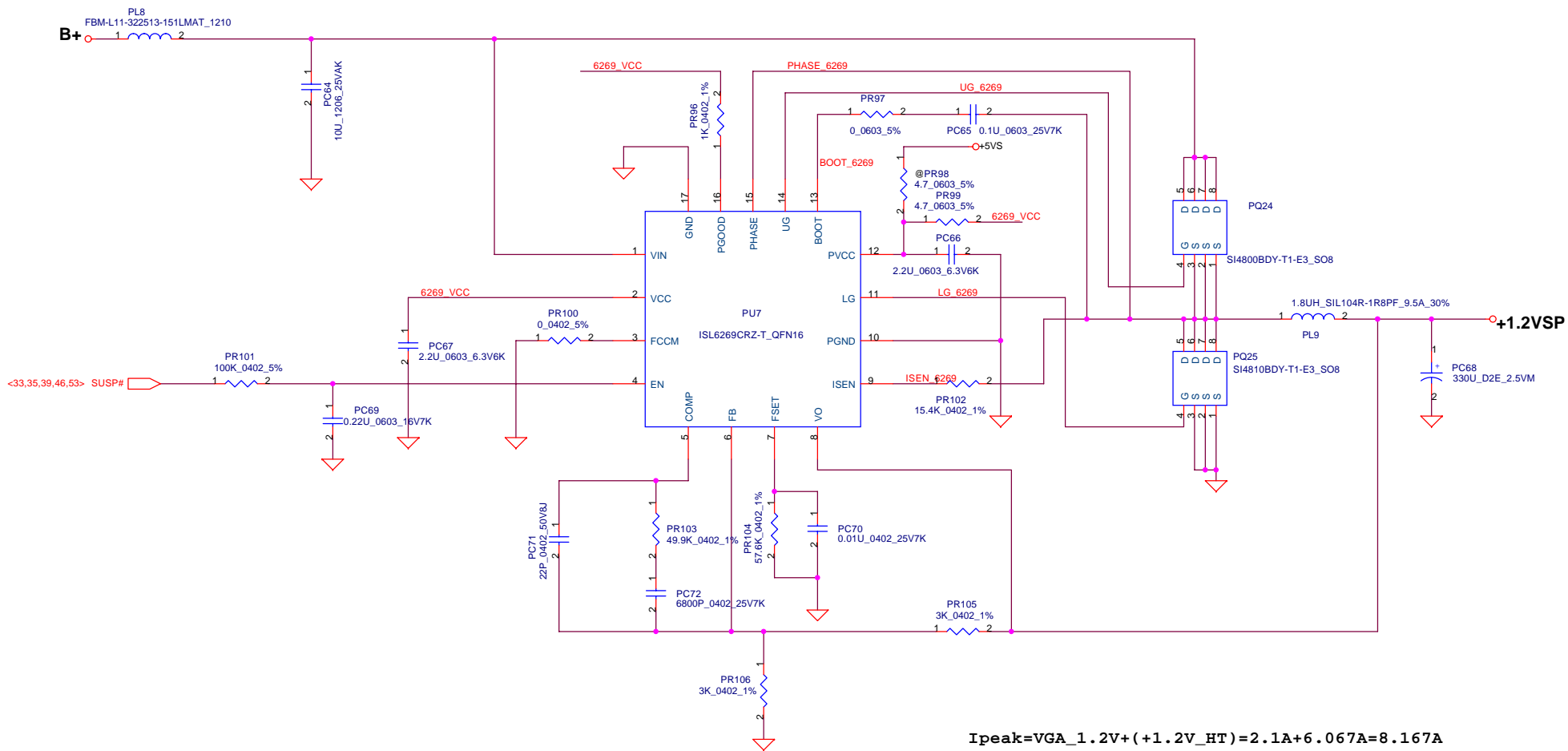
PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C



Vin Detector
Min. typ. Max.
H-->L 16.976V 17.257V 17.728V
L-->H 17.430V 17.901V 18.384V

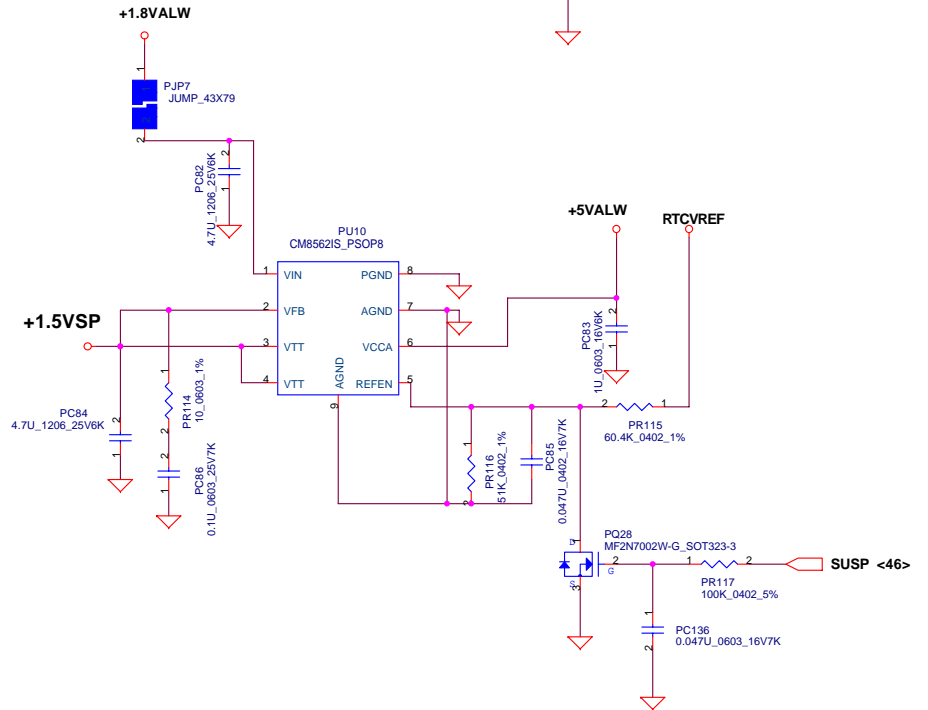
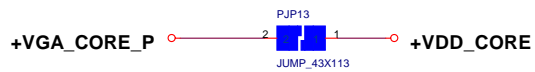
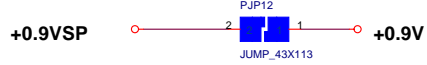
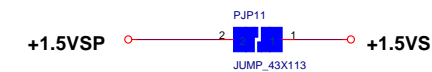
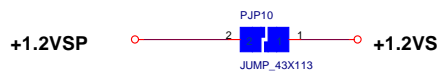
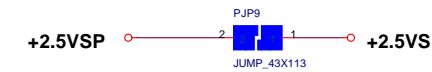
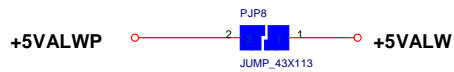
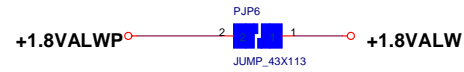
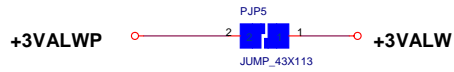
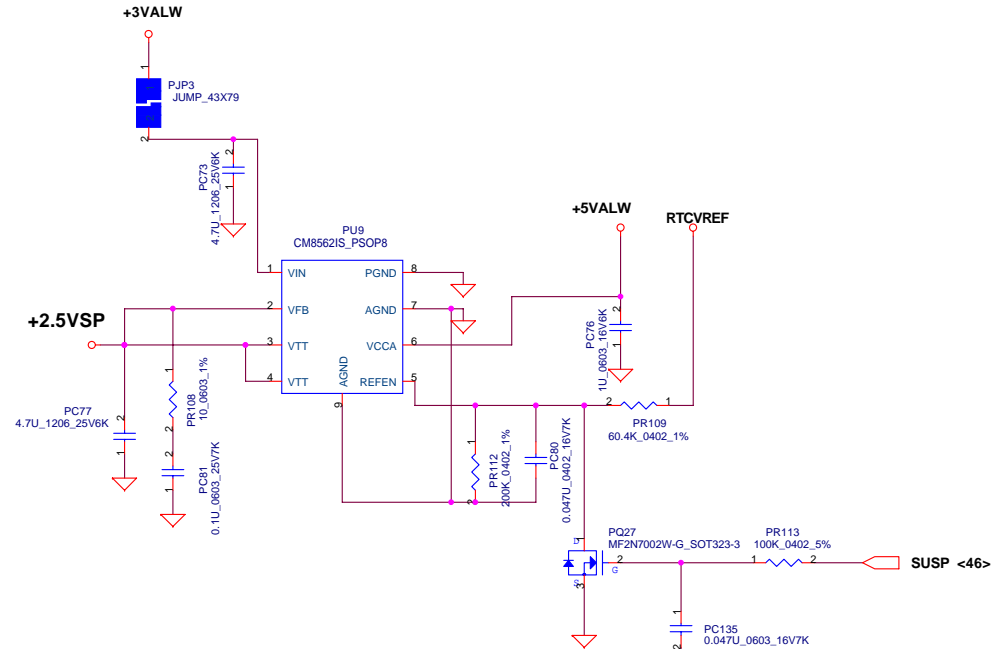
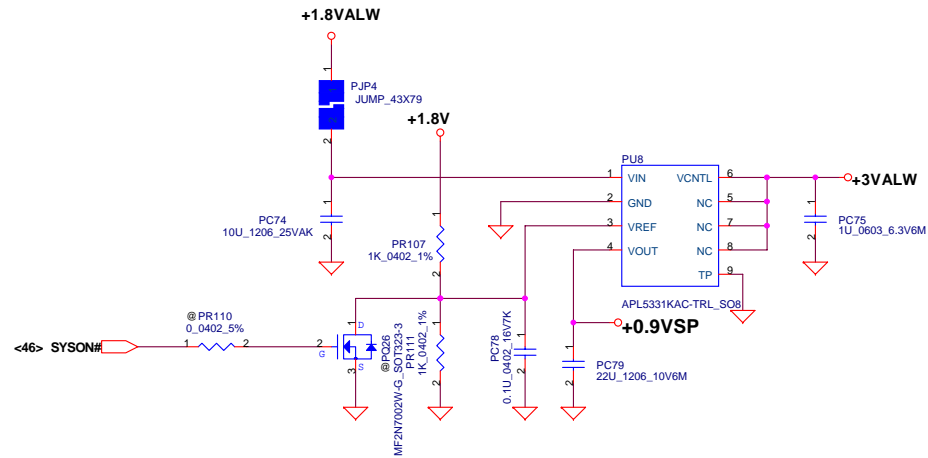


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$I_{peak} = V_{GA_1.2V} + (+1.2V_{HT}) = 2.1A + 6.067A = 8.167A$
 $I_{max} = 5.7A$
 $I_{ocmin} = 9.23A$
 $I_{ocmax} = 19.23A$

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